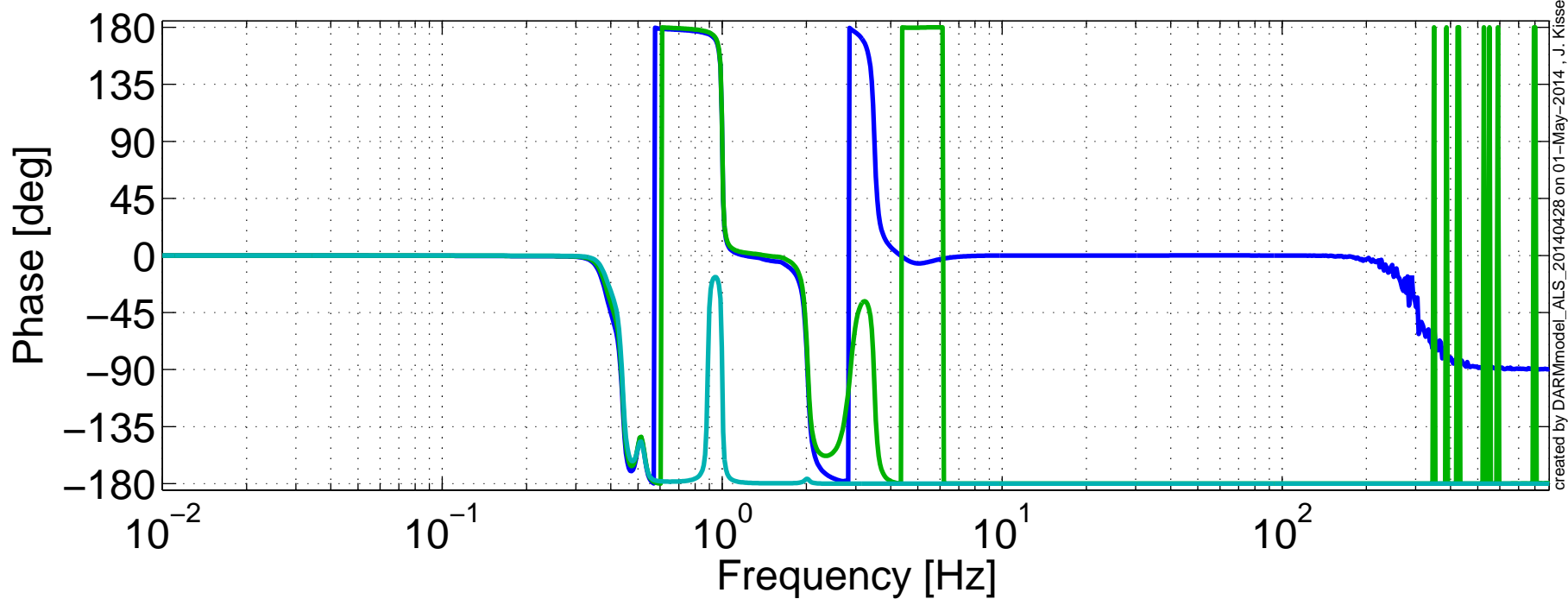
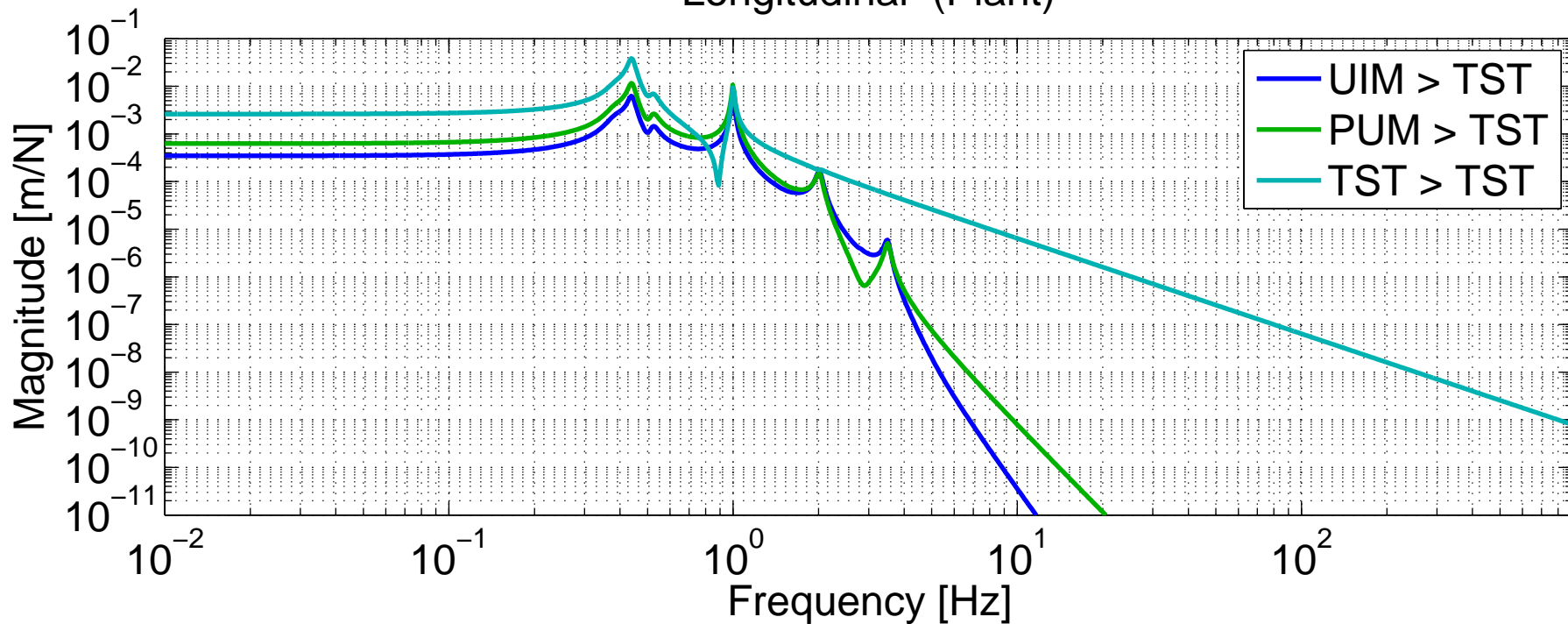
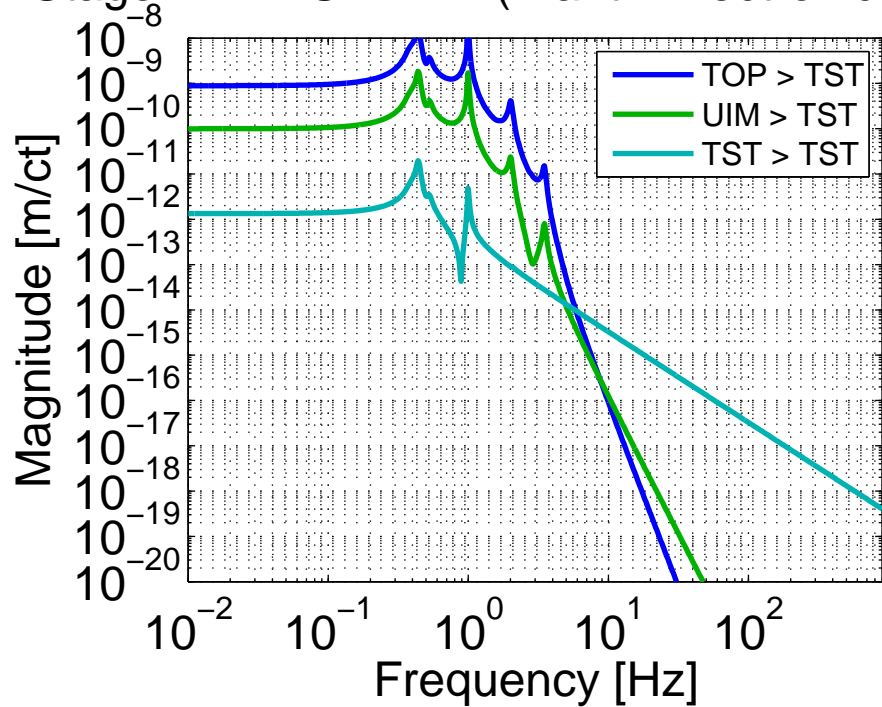


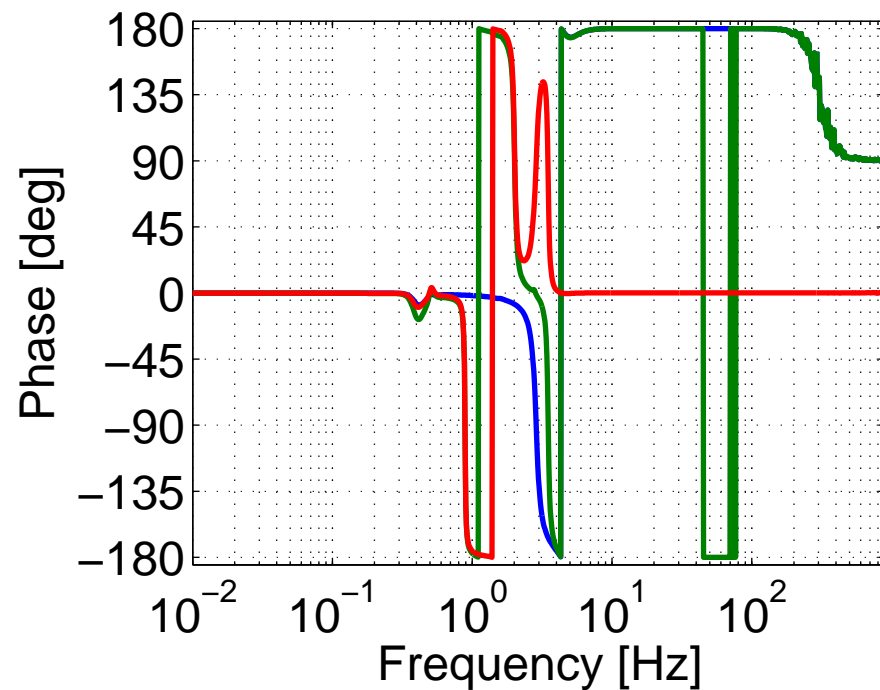
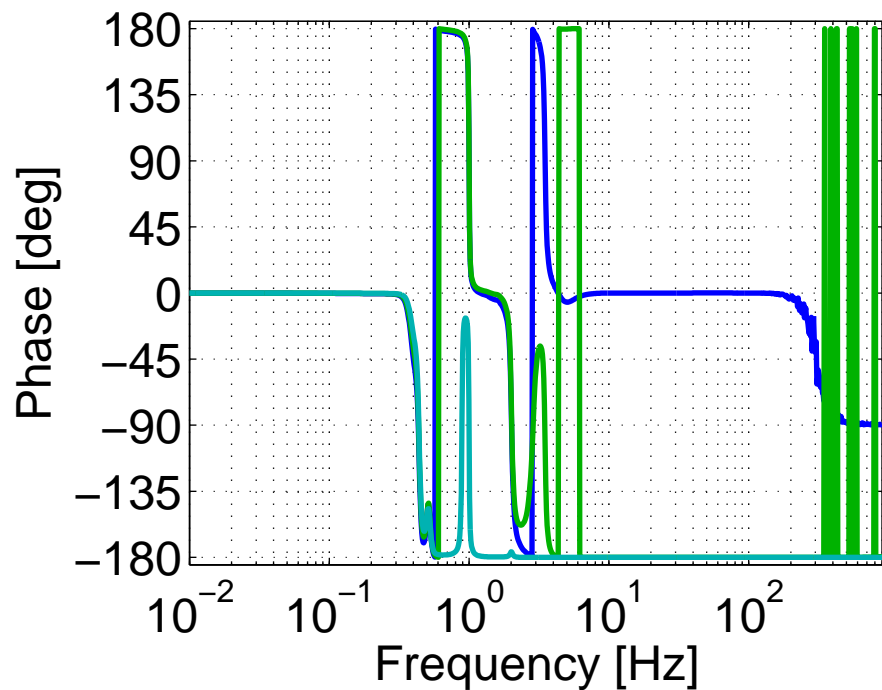
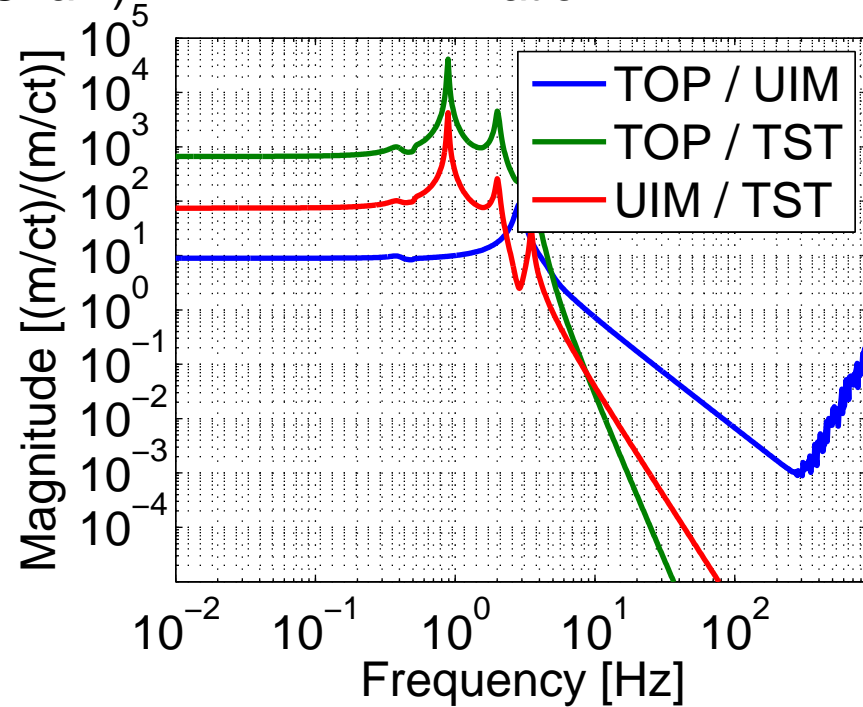
Damped QUAD IStage > IST Transfer Function Longitudinal (Plant)



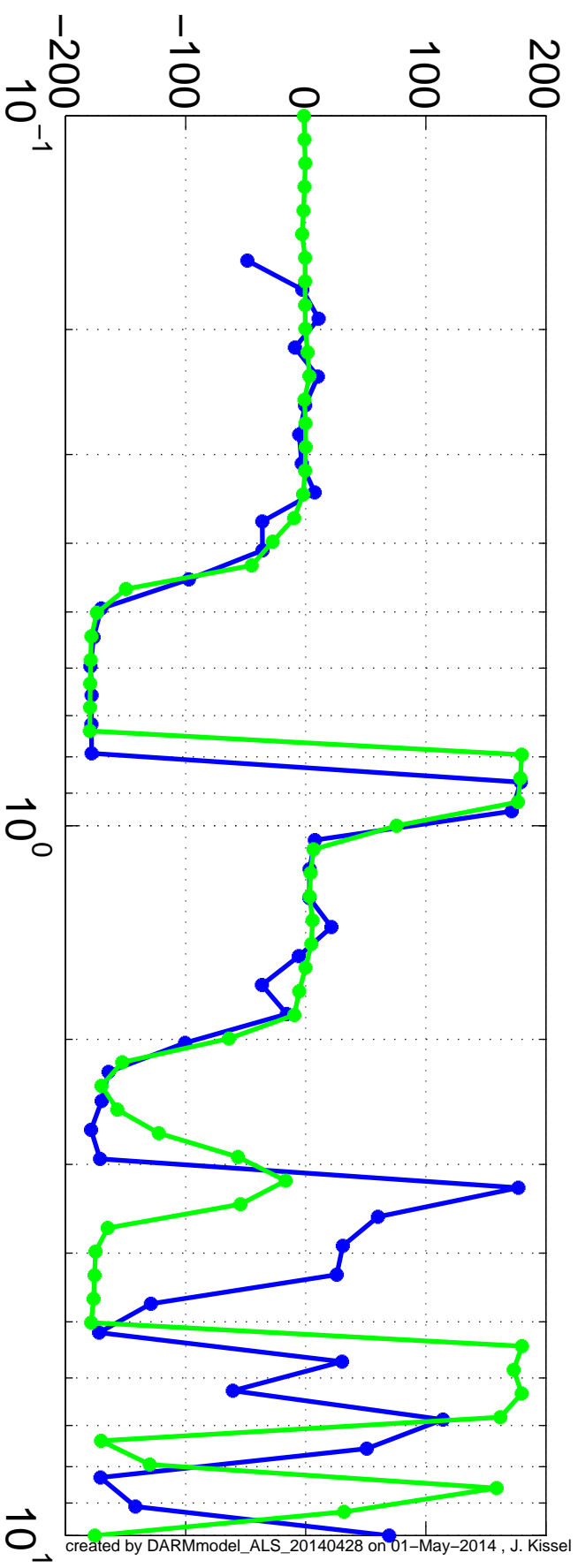
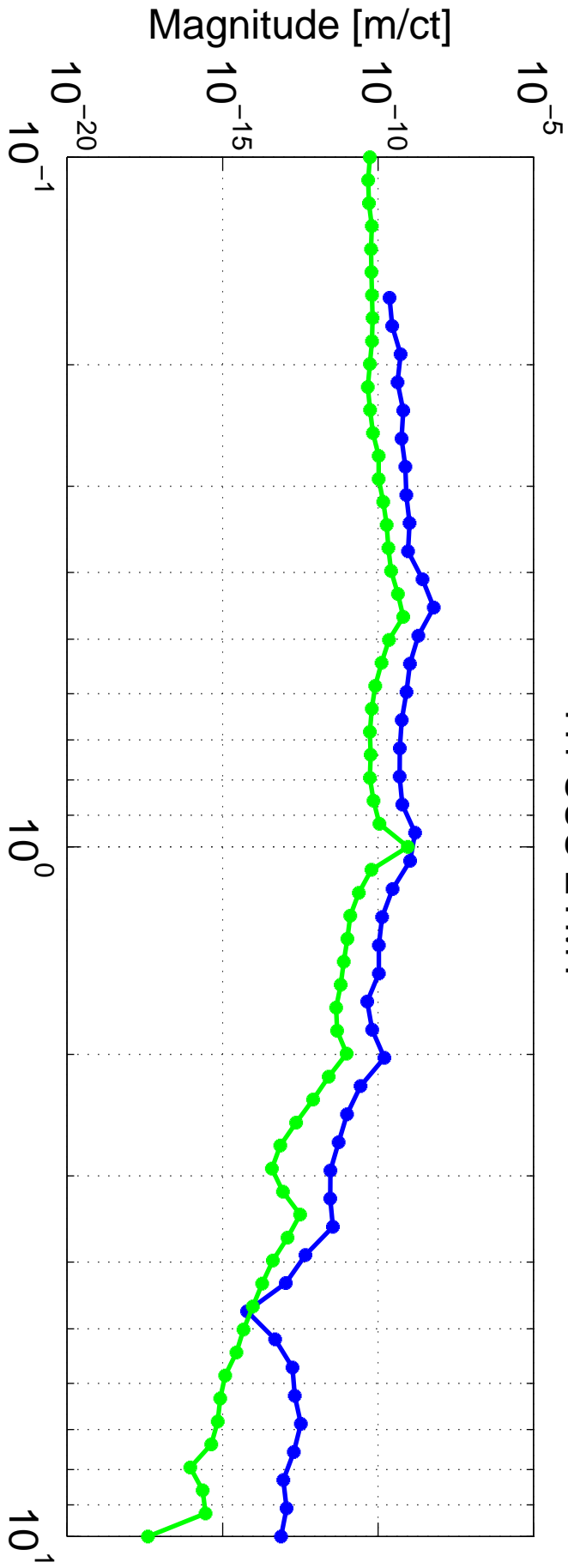
iStage L -> TST L TF (Plant * Electronics Chain)



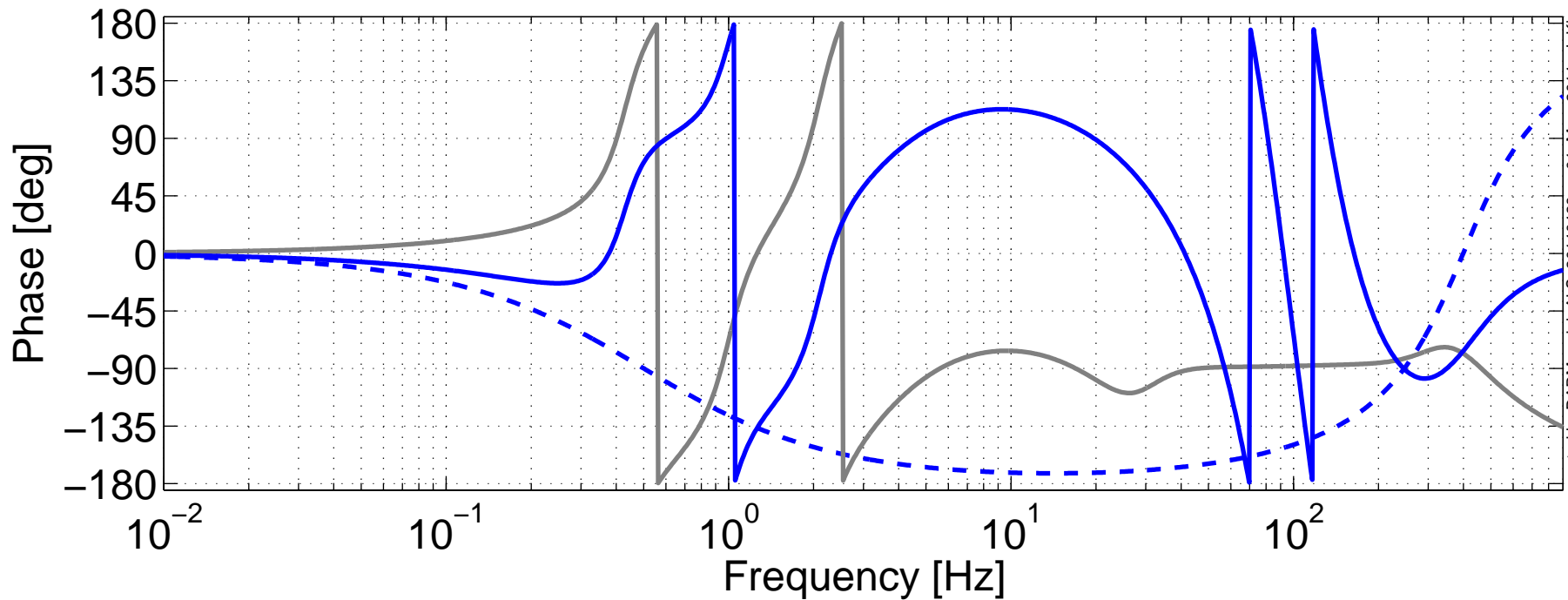
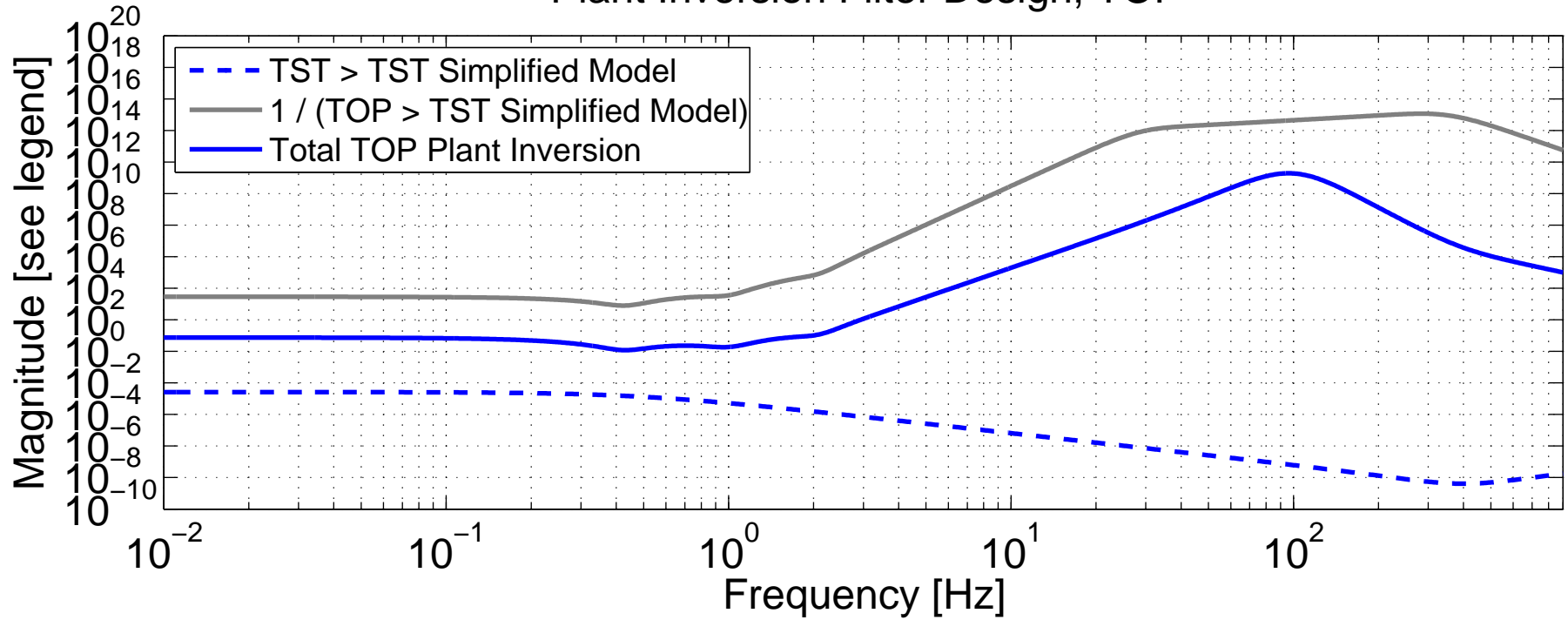
Ratio



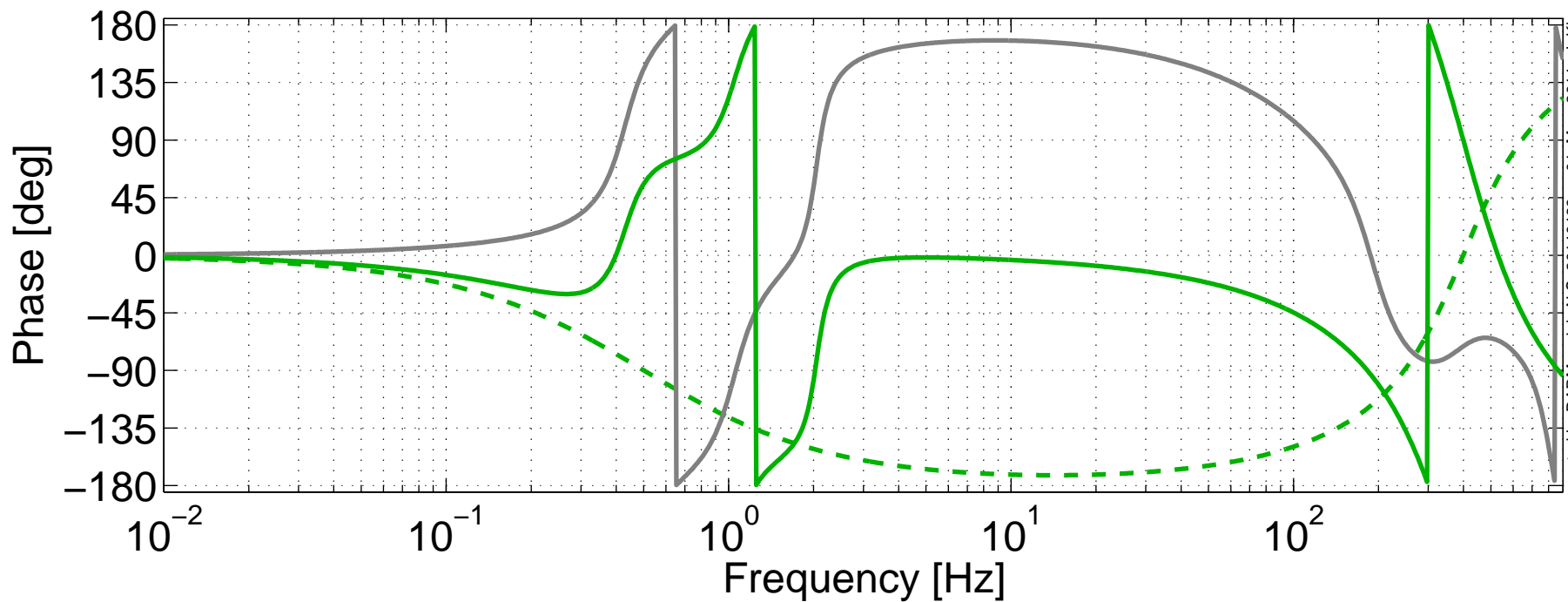
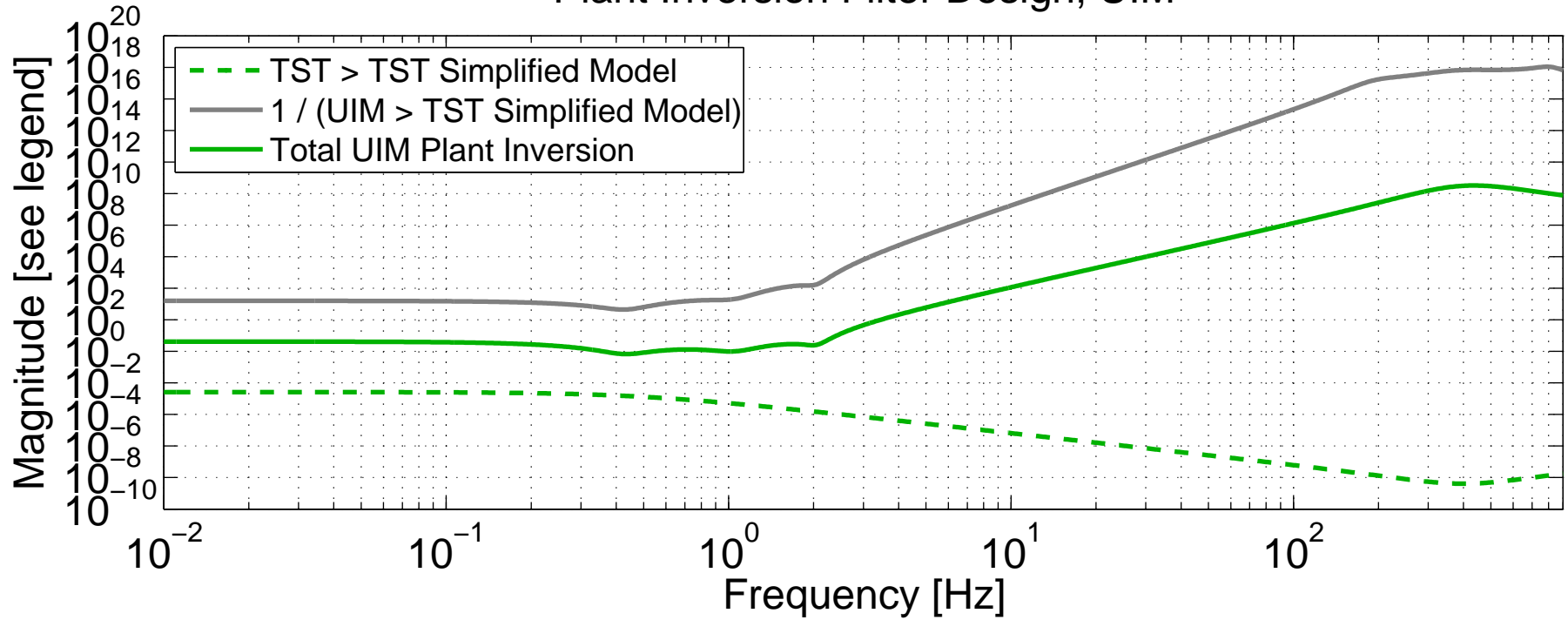
H1 SUS ETMY



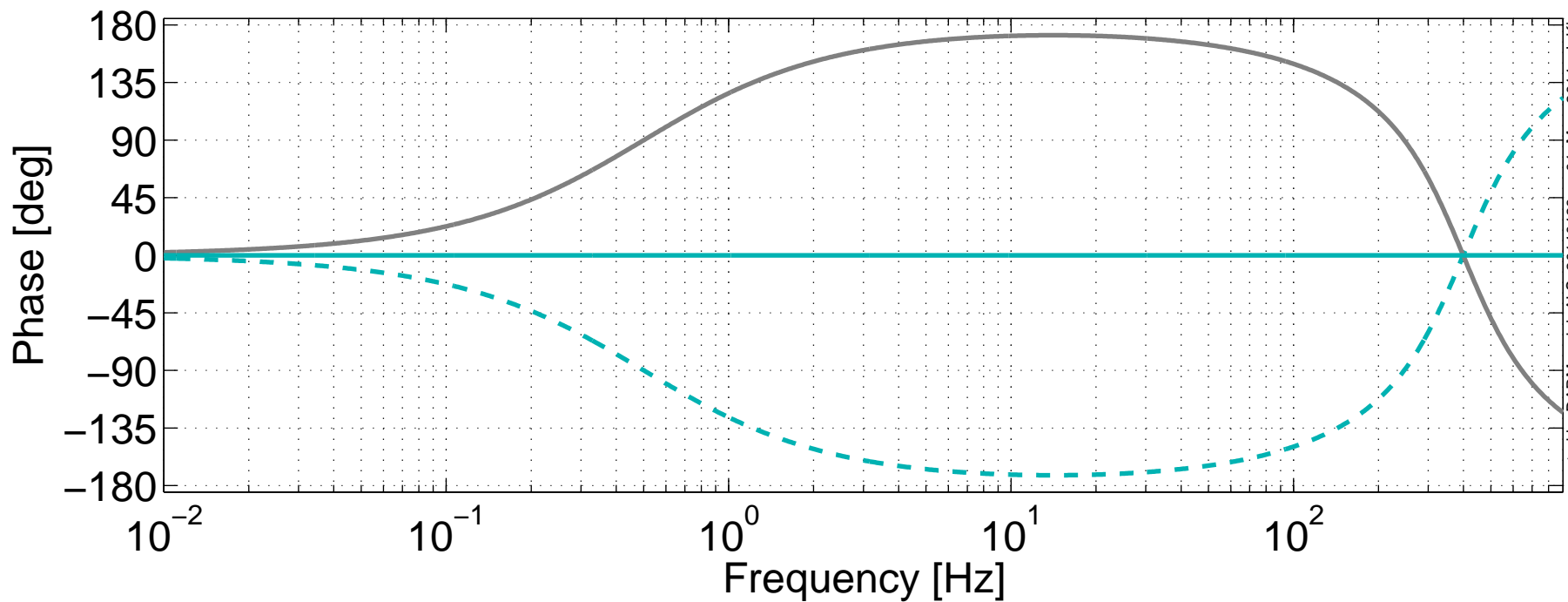
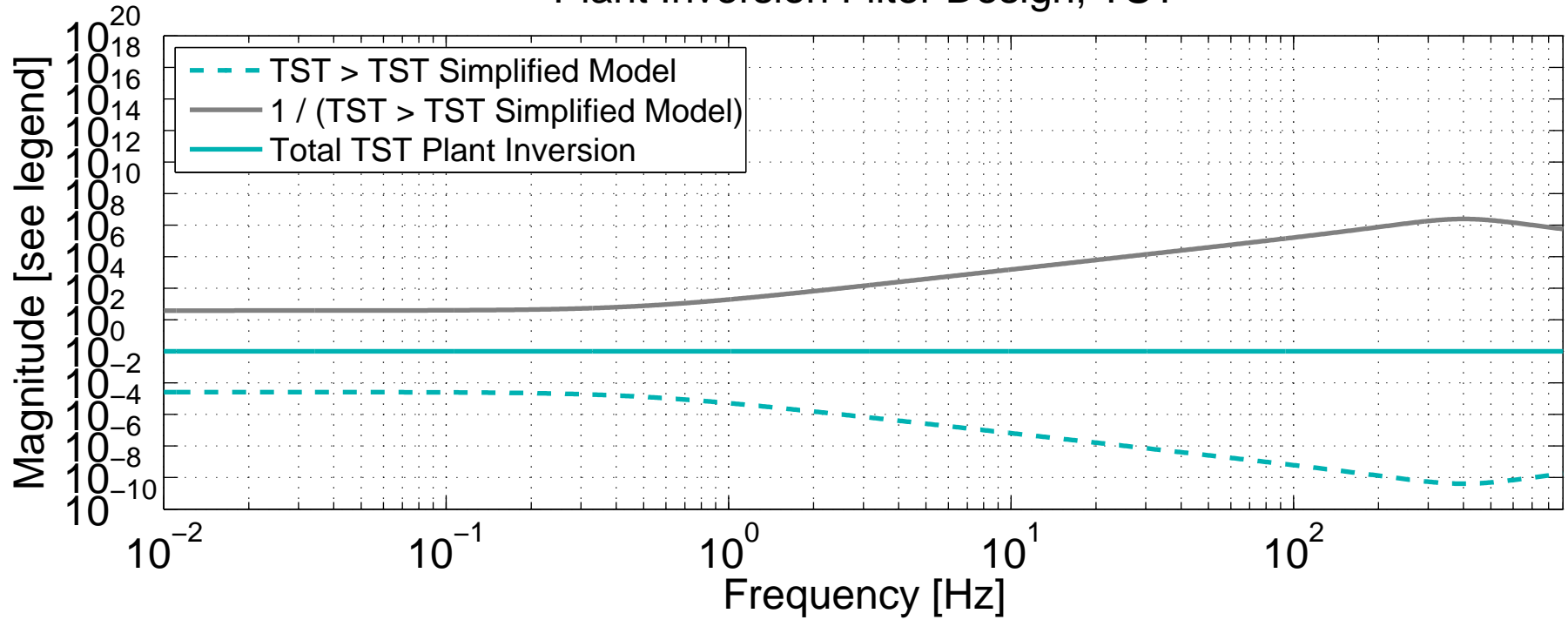
Plant Inversion Filter Design, TOP



Plant Inversion Filter Design, UIM

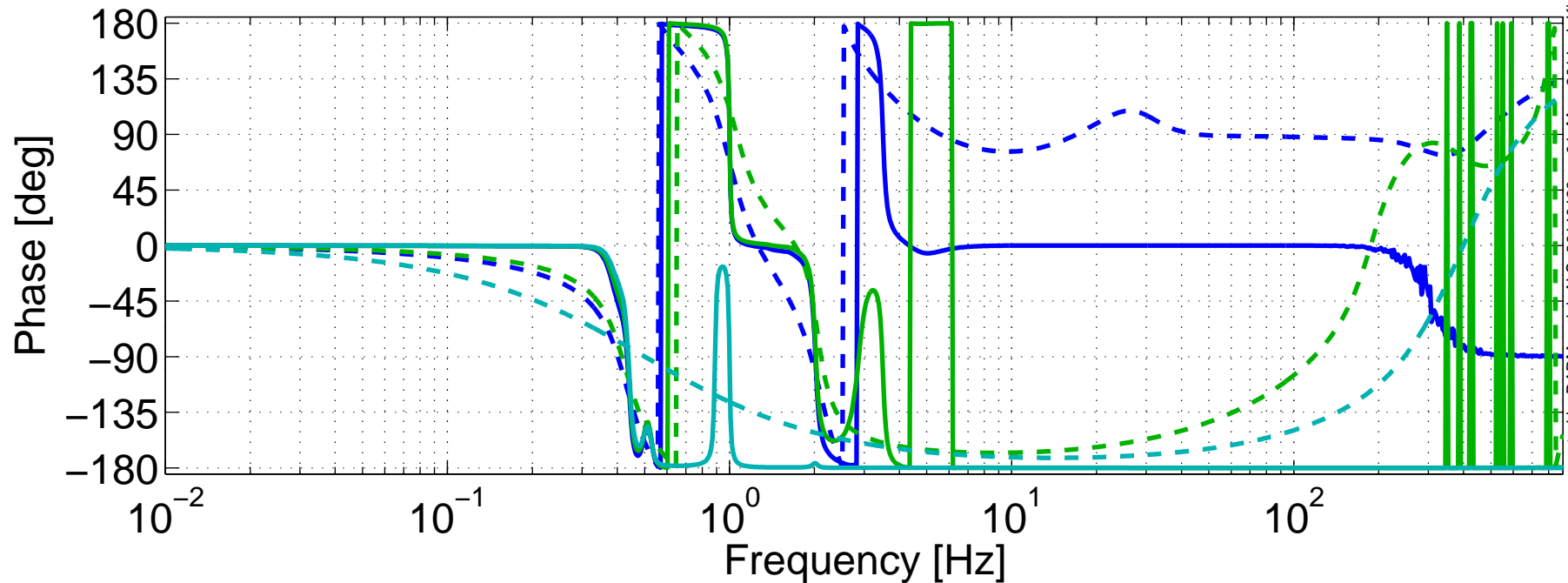
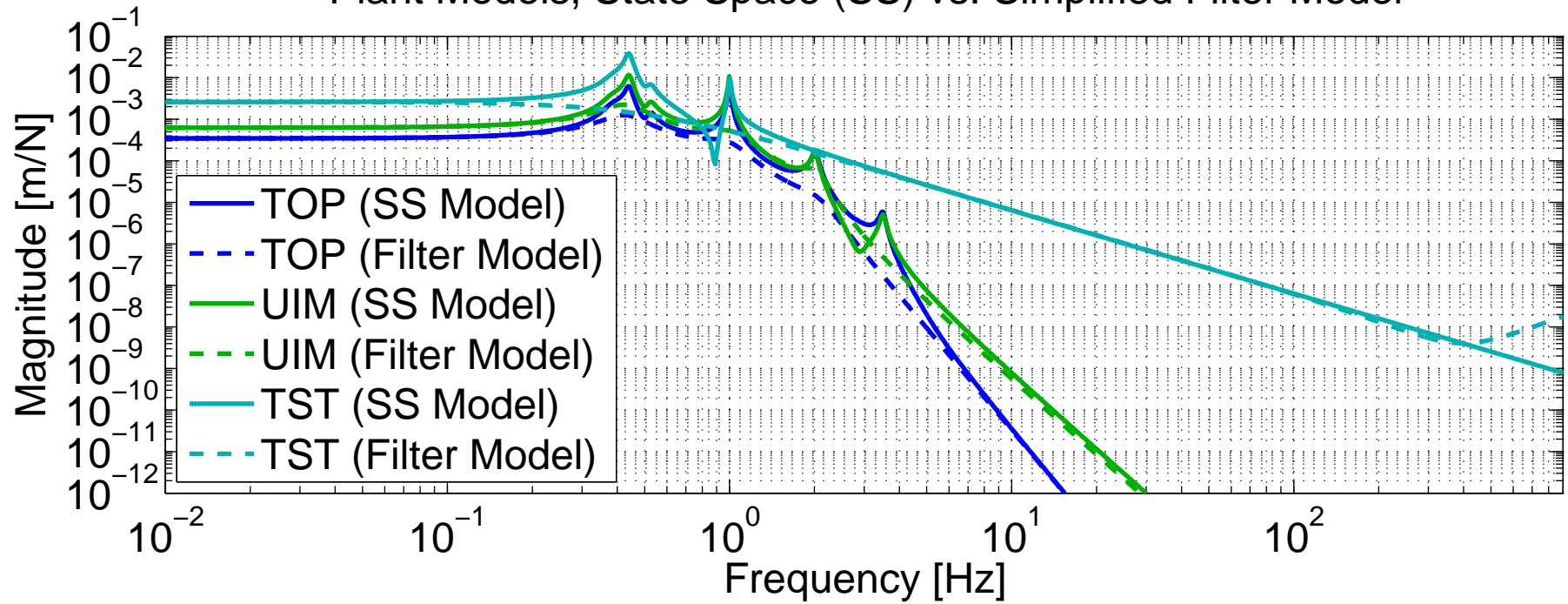


Plant Inversion Filter Design, TST

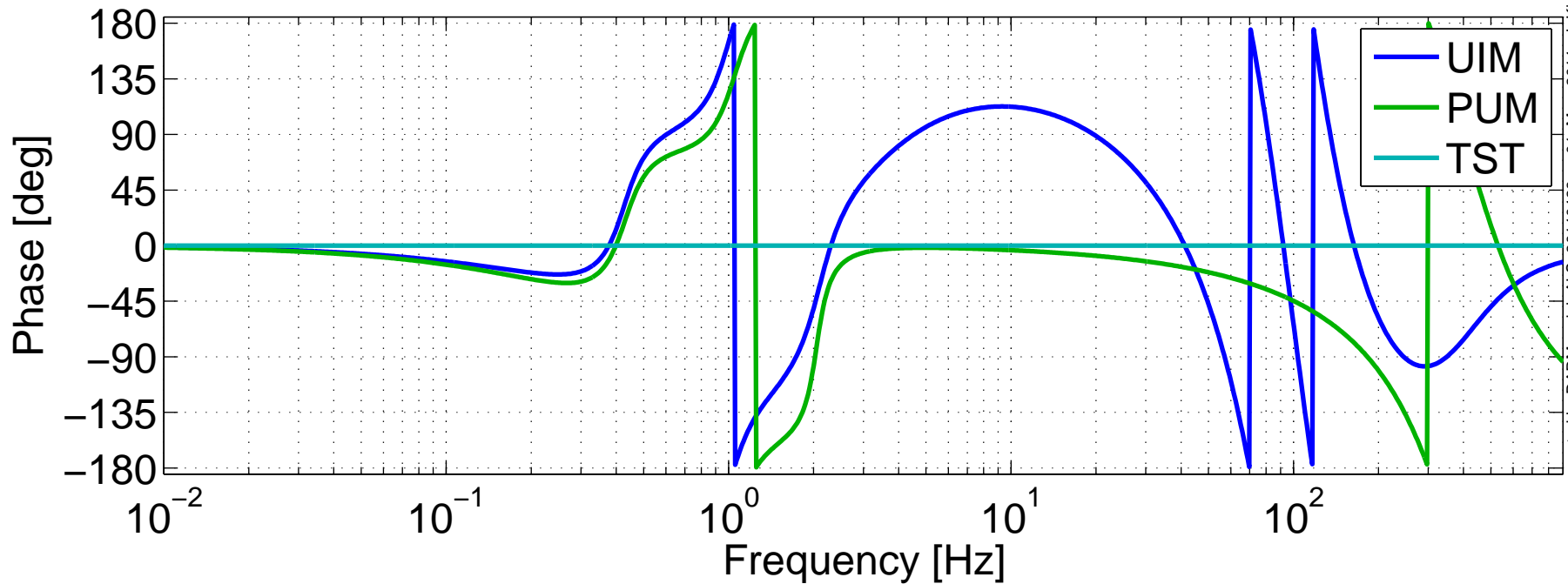
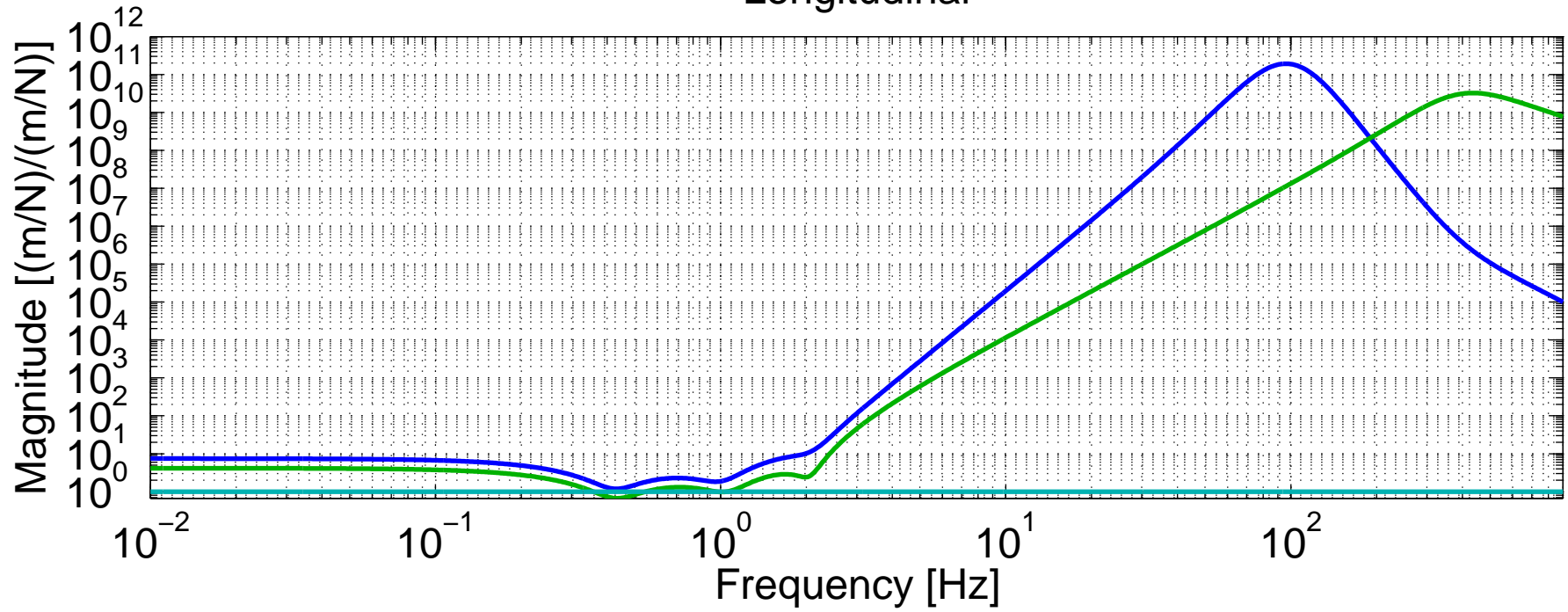


Plant Inversion Filter Design

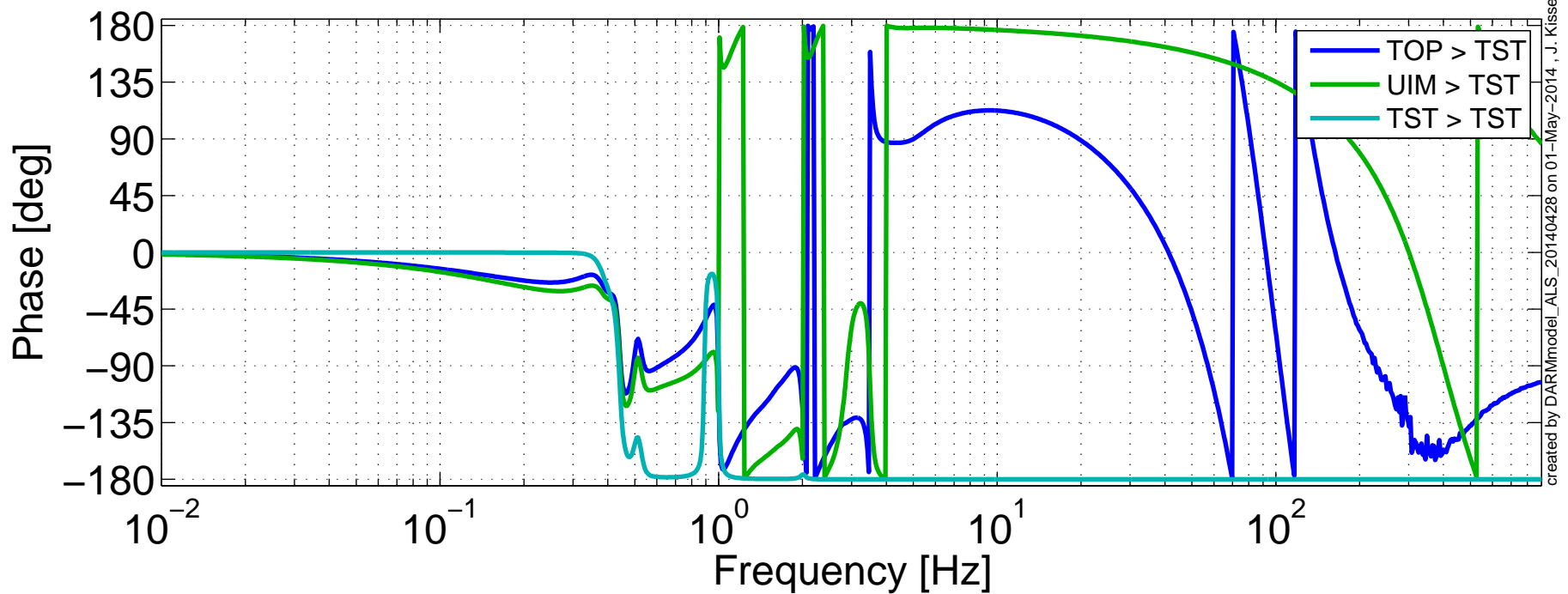
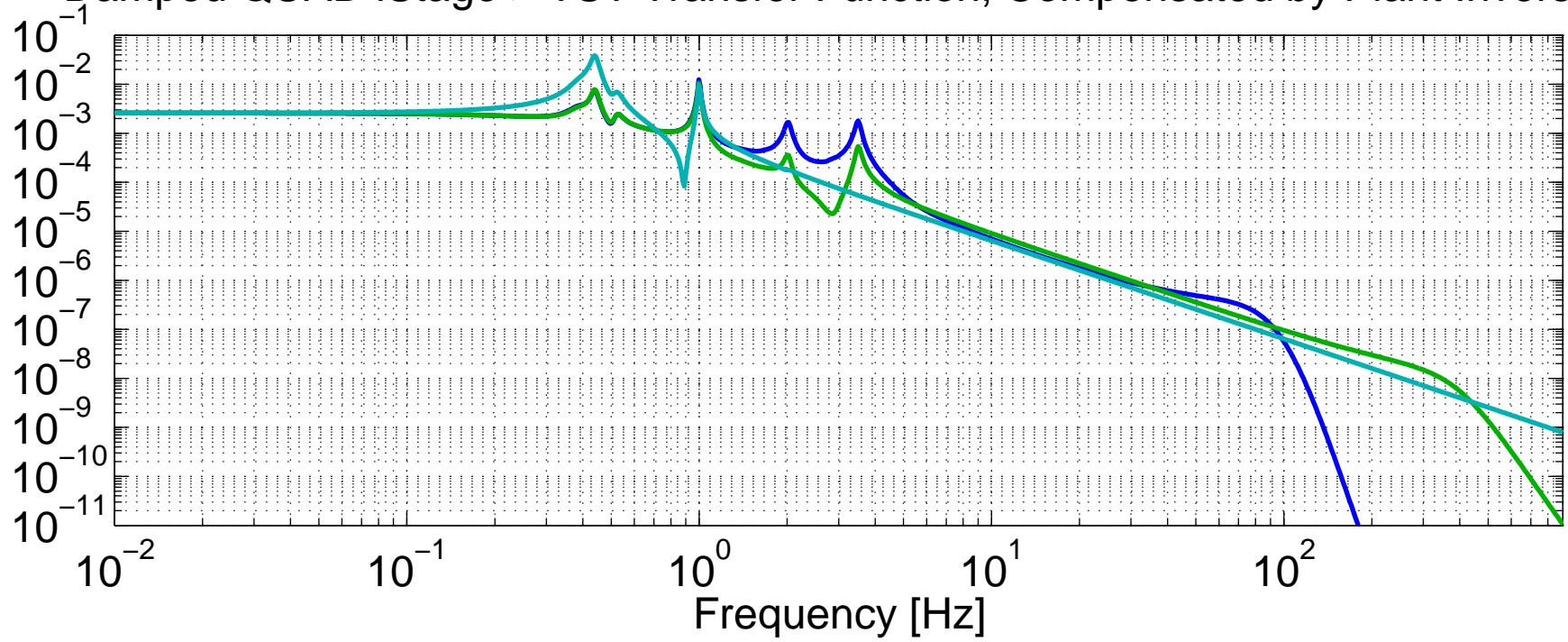
Plant Models, State Space (SS) vs. Simplified Filter Model



Plant Inversion Filters Longitudinal

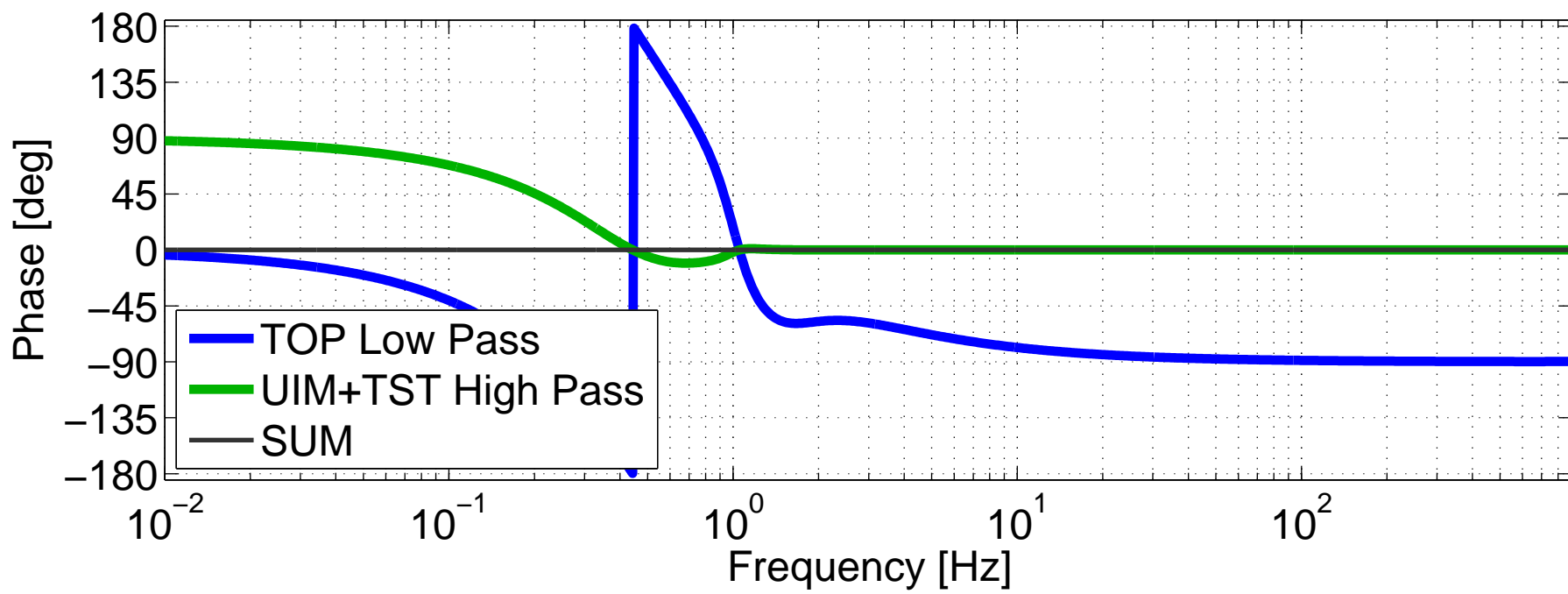
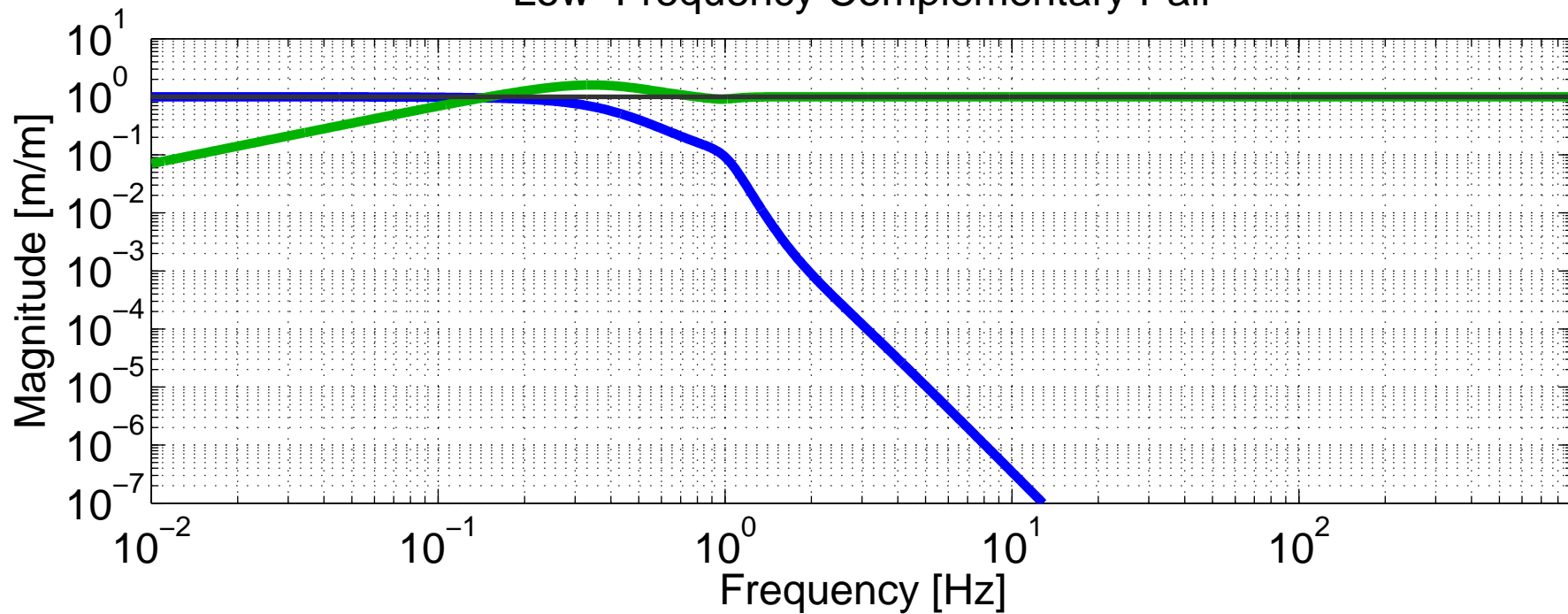


Damped QUAD iStage > TST Transfer Function, Compensated by Plant Inversion



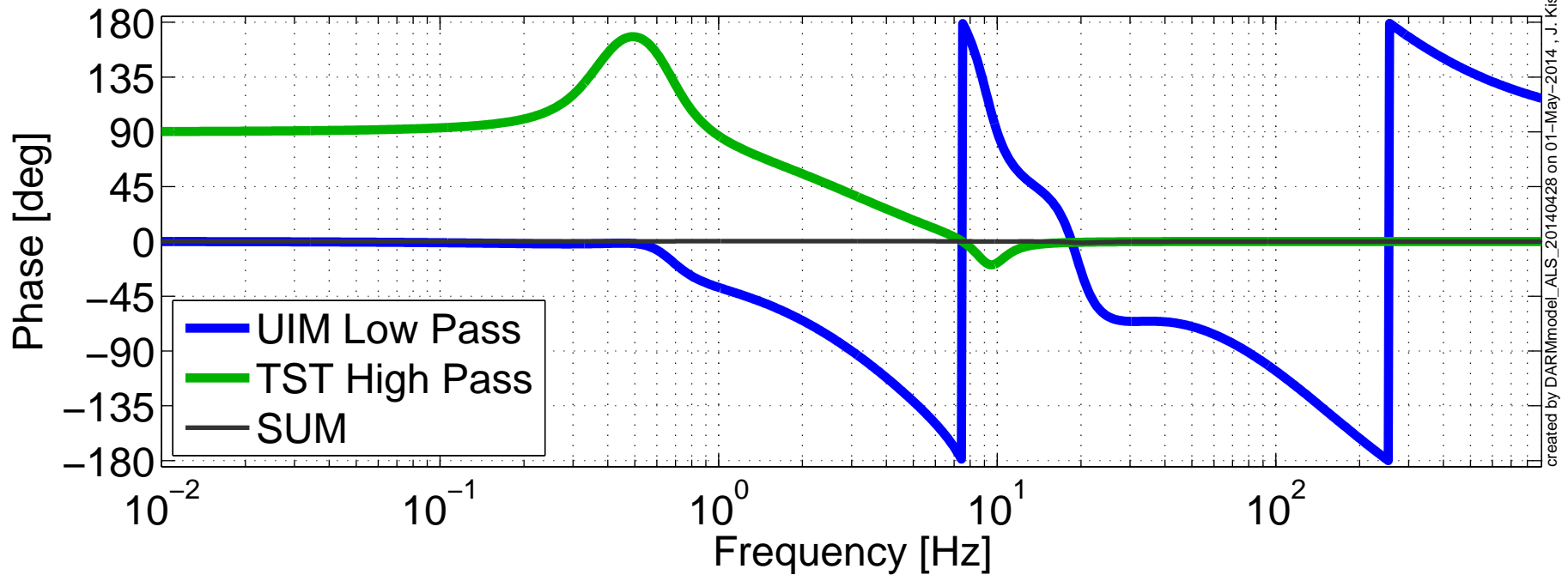
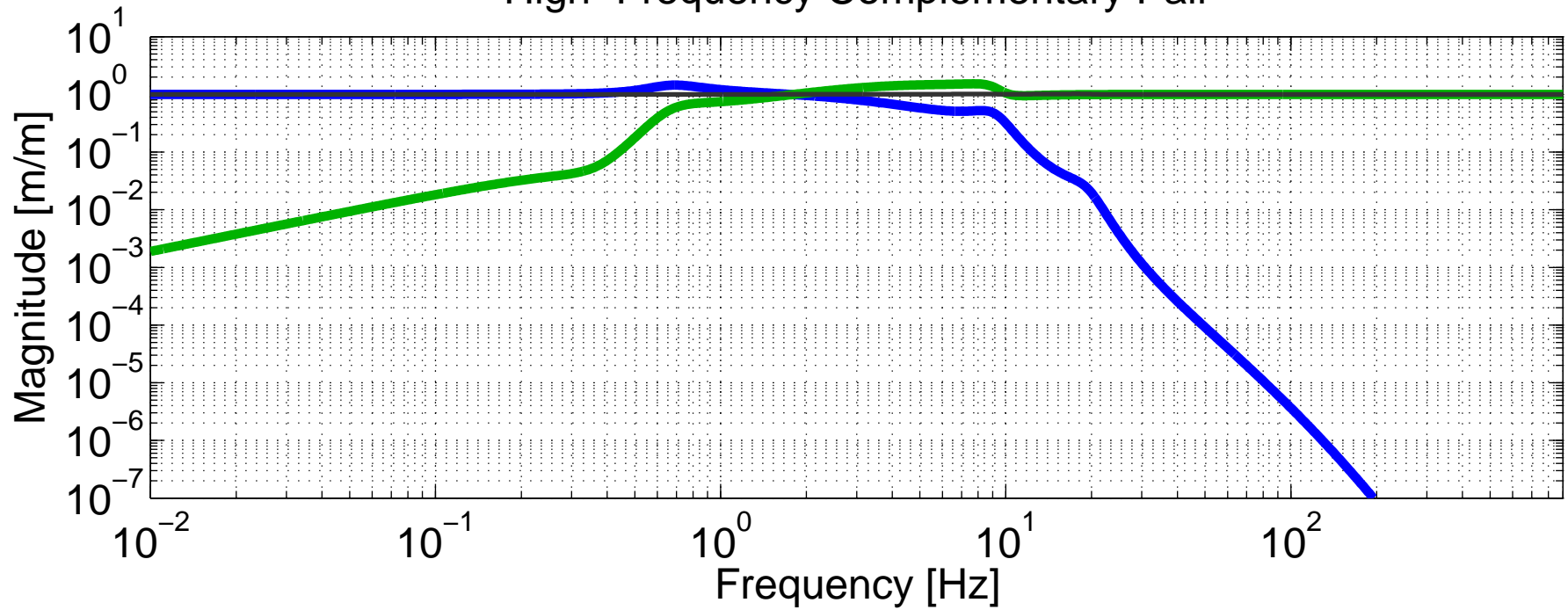
Distribution Filter Design

Low-Frequency Complementary Pair



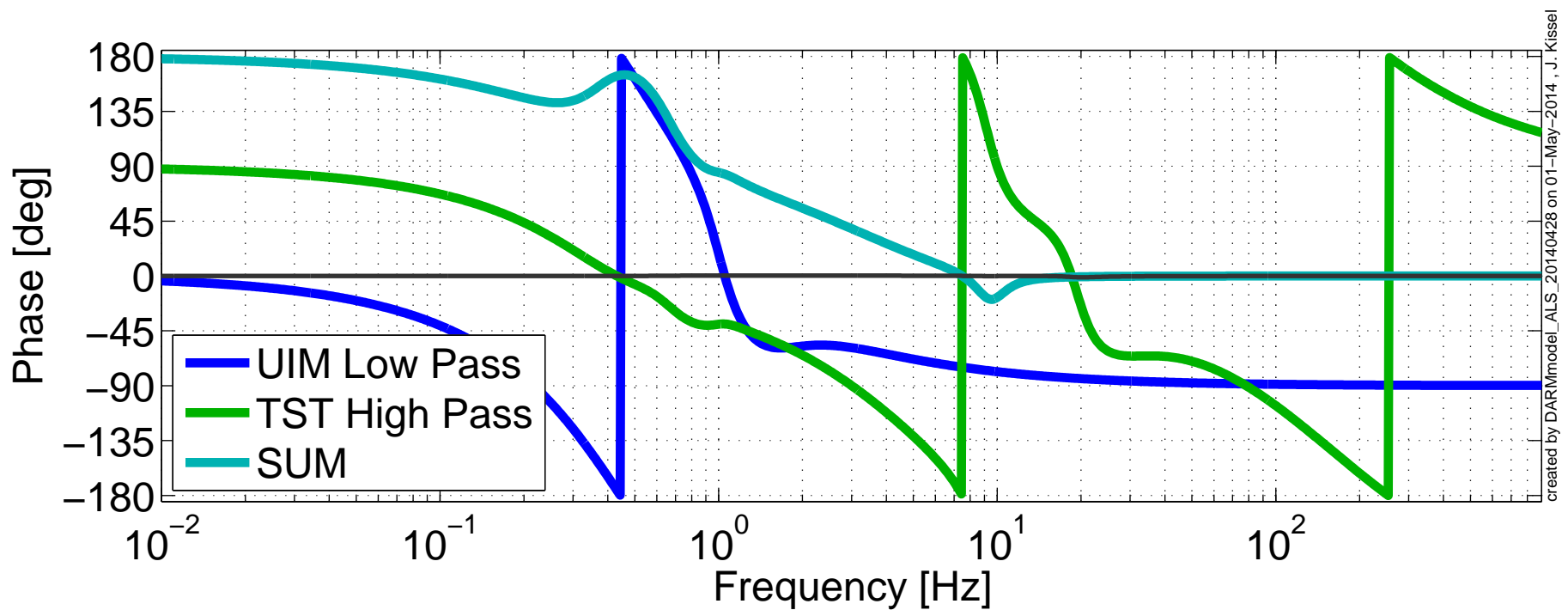
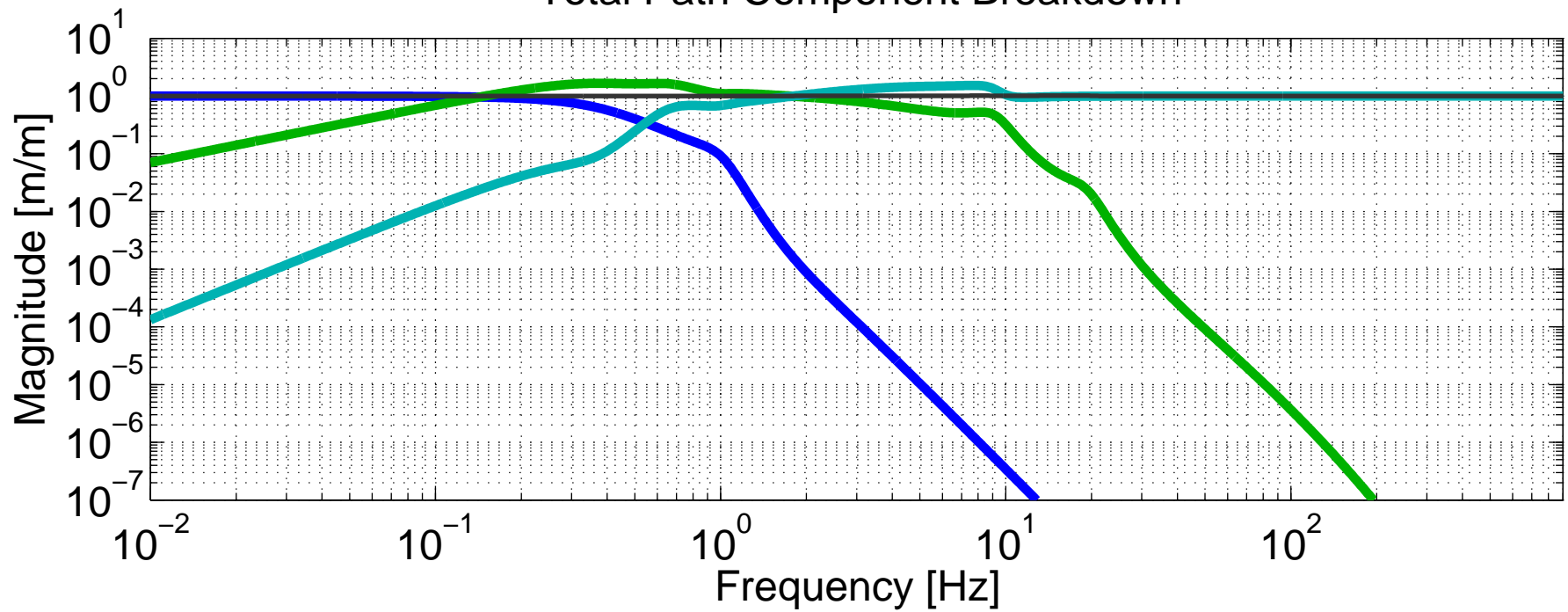
Distribution Filter Design

High-Frequency Complementary Pair

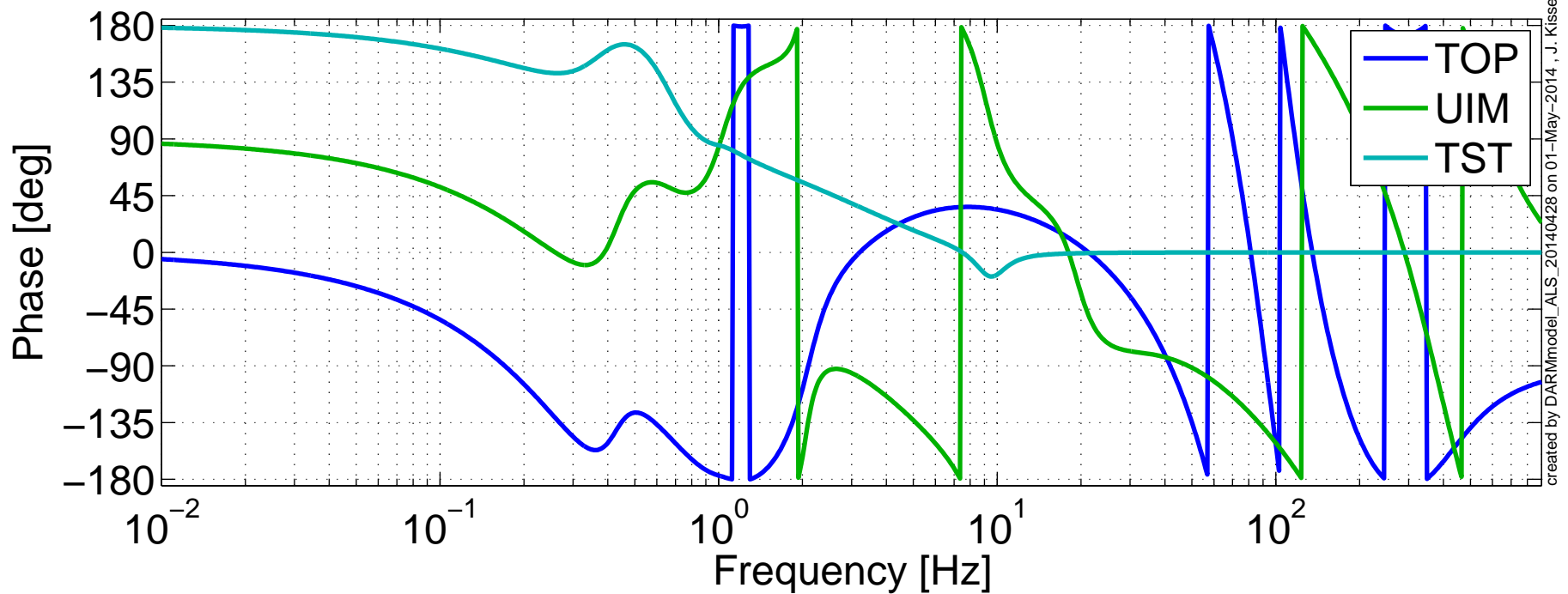
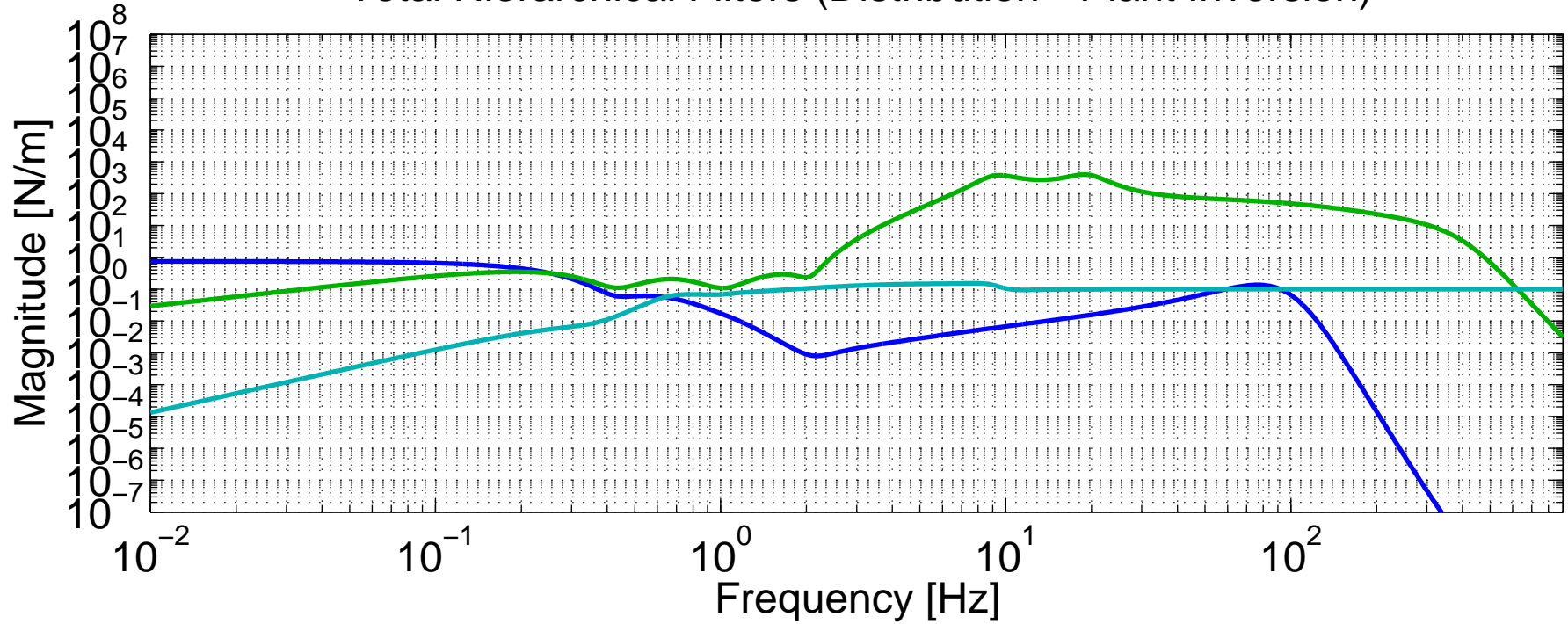


Distribution Filter Design

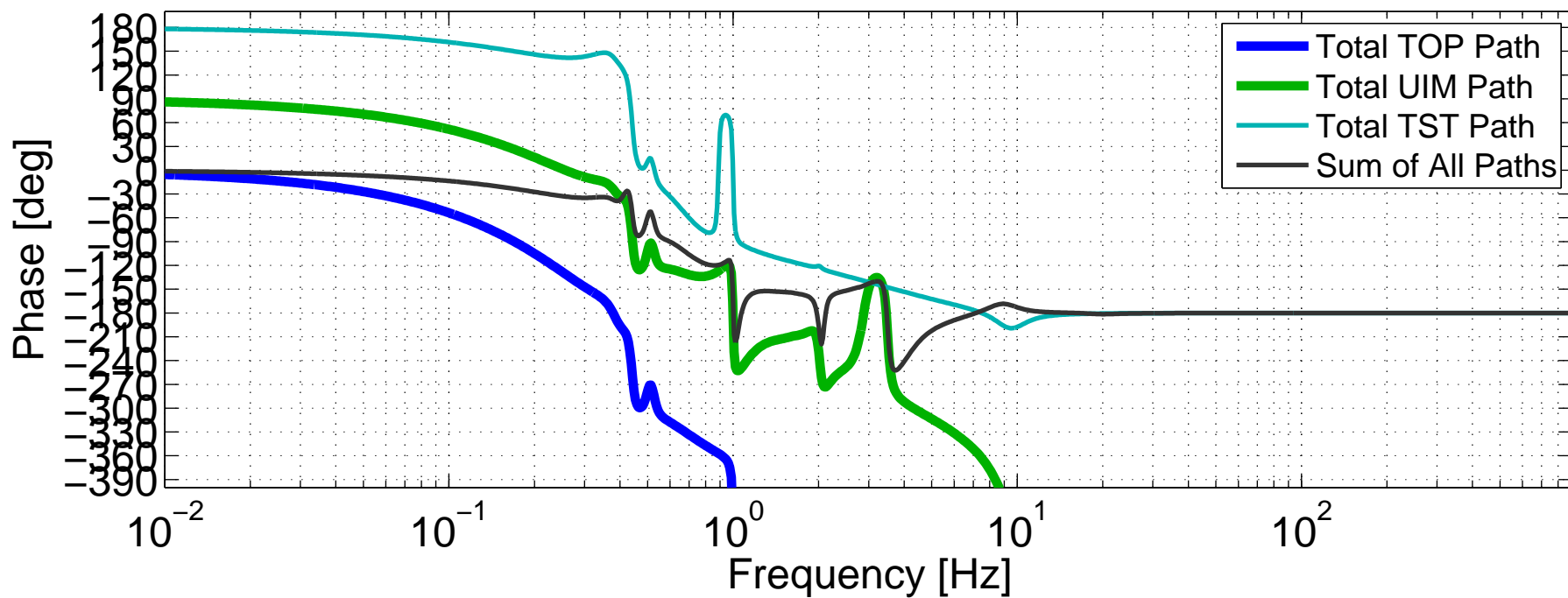
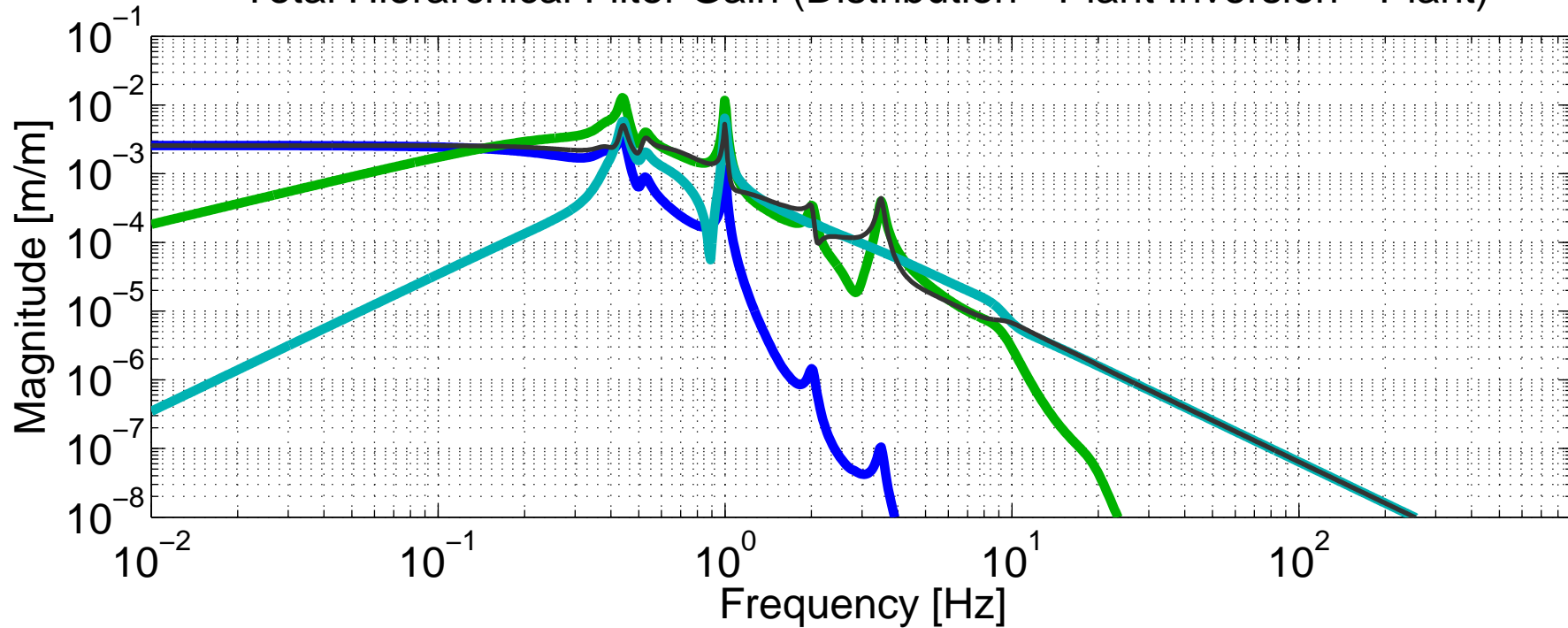
Total Path Component Breakdown



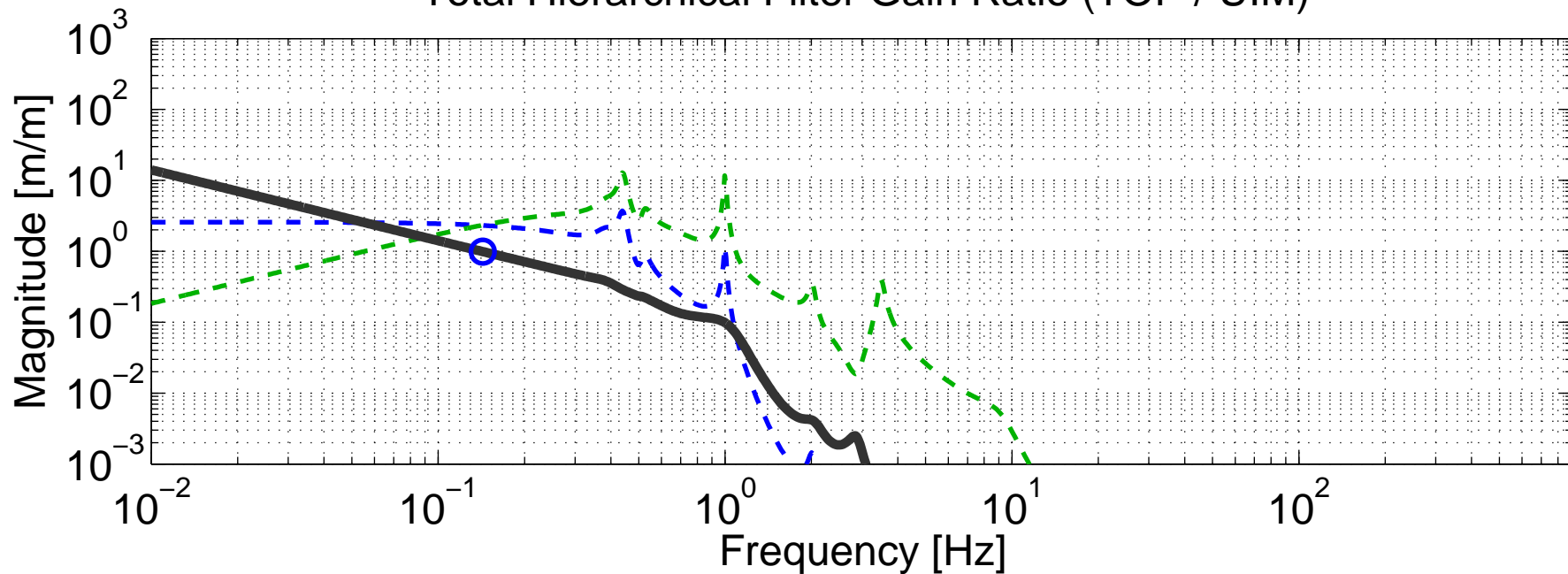
Total Hierarchical Filters (Distribution * Plant Inversion)



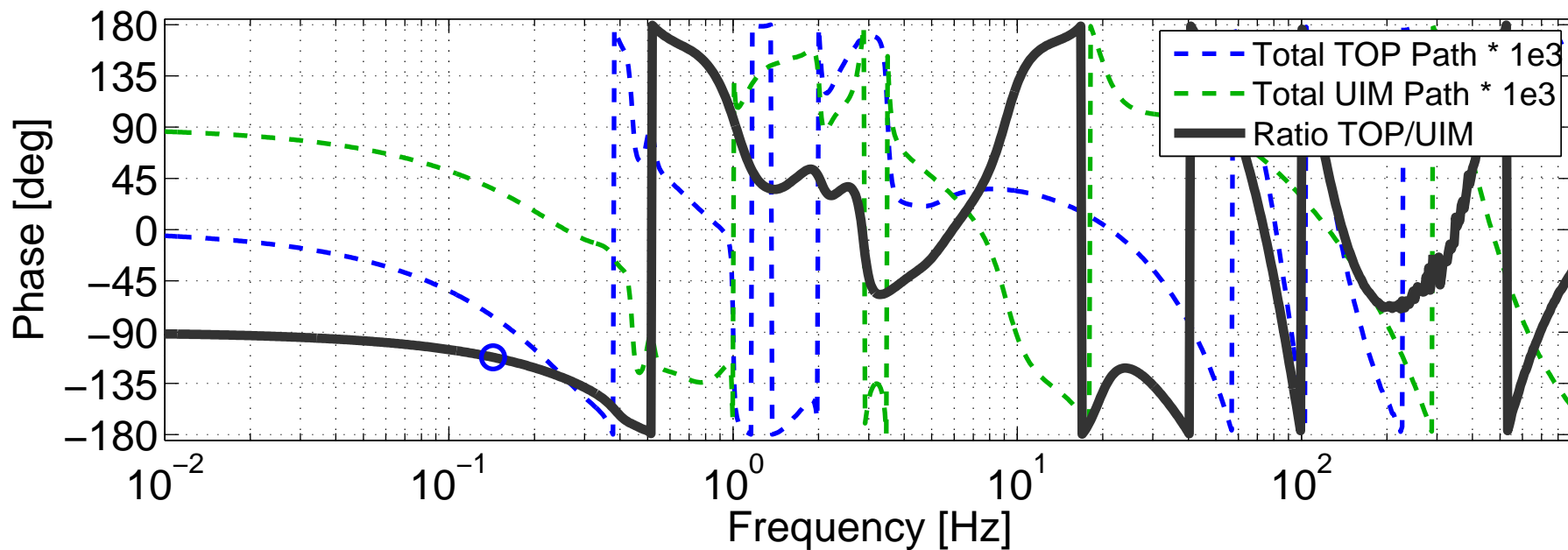
Total Hierarchical Filter Gain (Distribution * Plant Inversion * Plant)



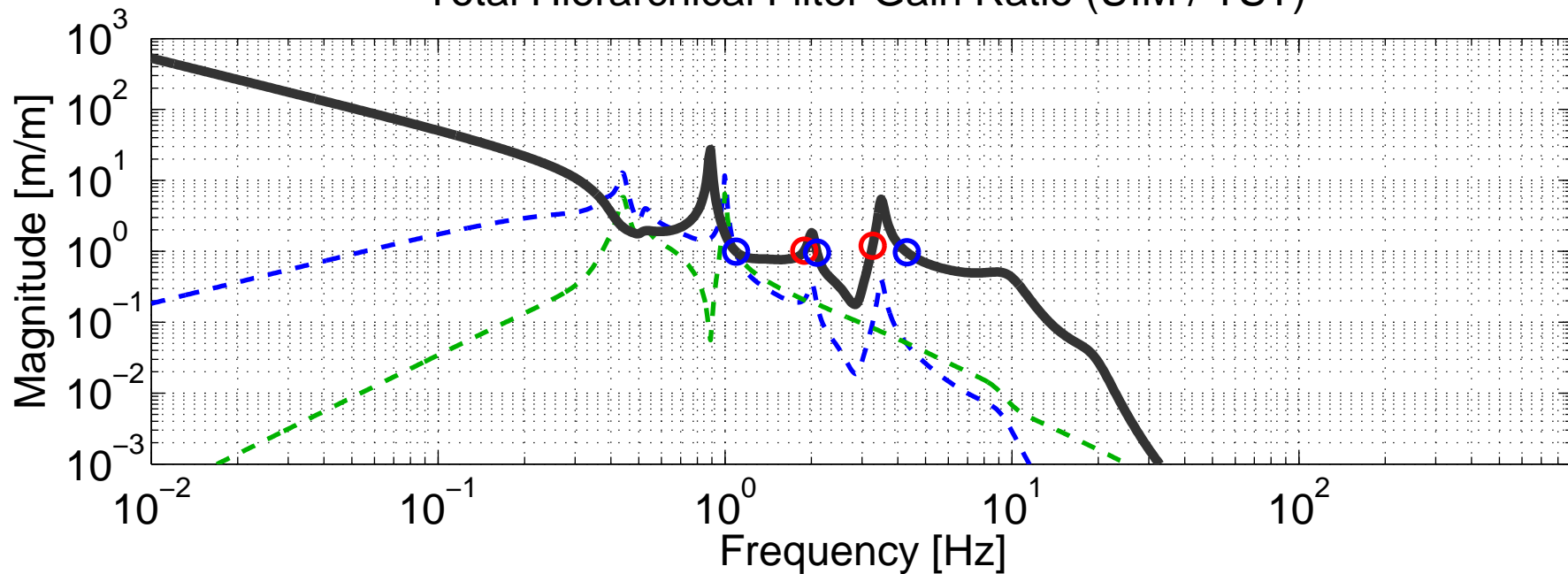
Total Hierarchical Filter Gain Ratio (TOP / UIM)



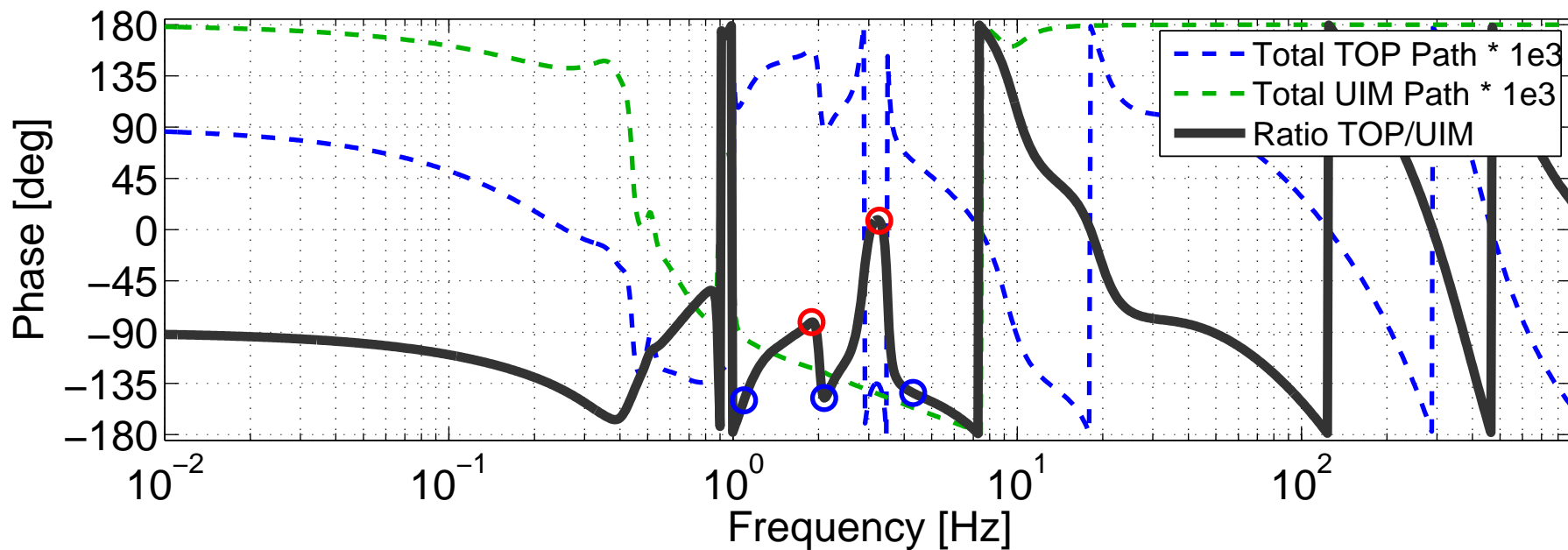
LUGF Phase Margins (red): [] [deg]
UUGF Phase Margins (blue): [67.9] [deg]



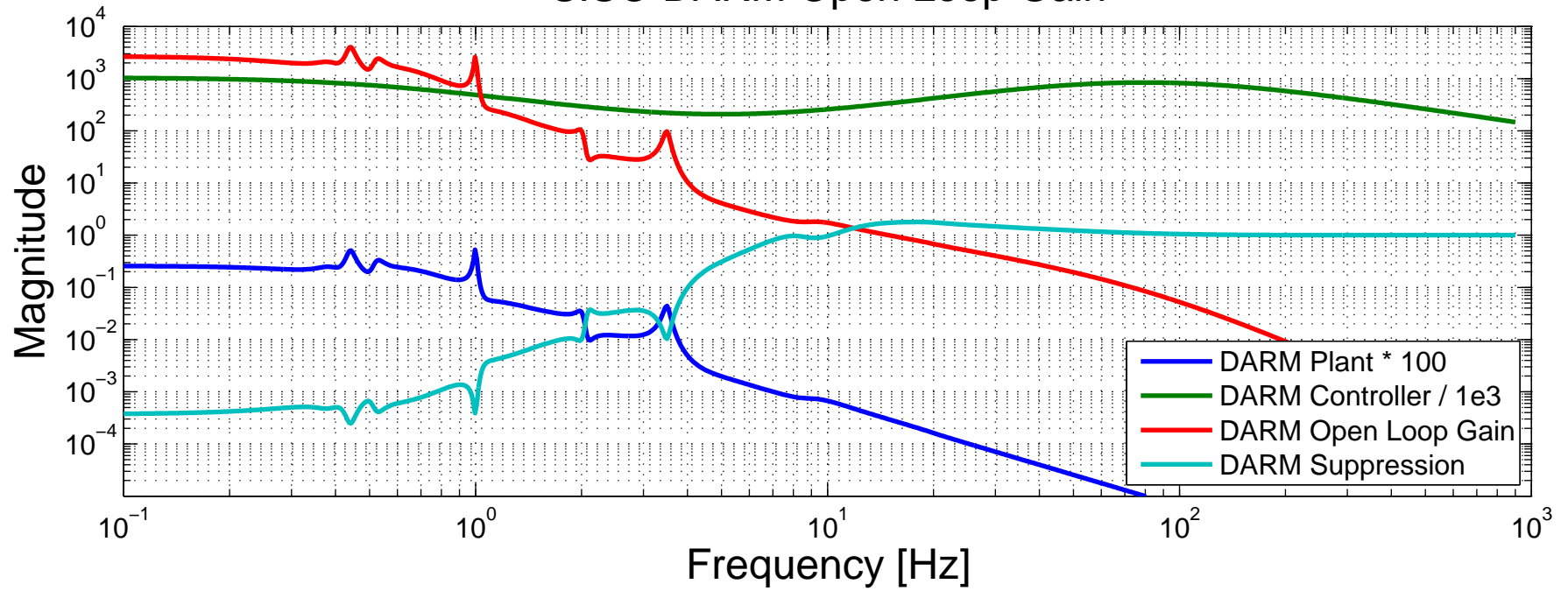
Total Hierarchical Filter Gain Ratio (UIM / TST)



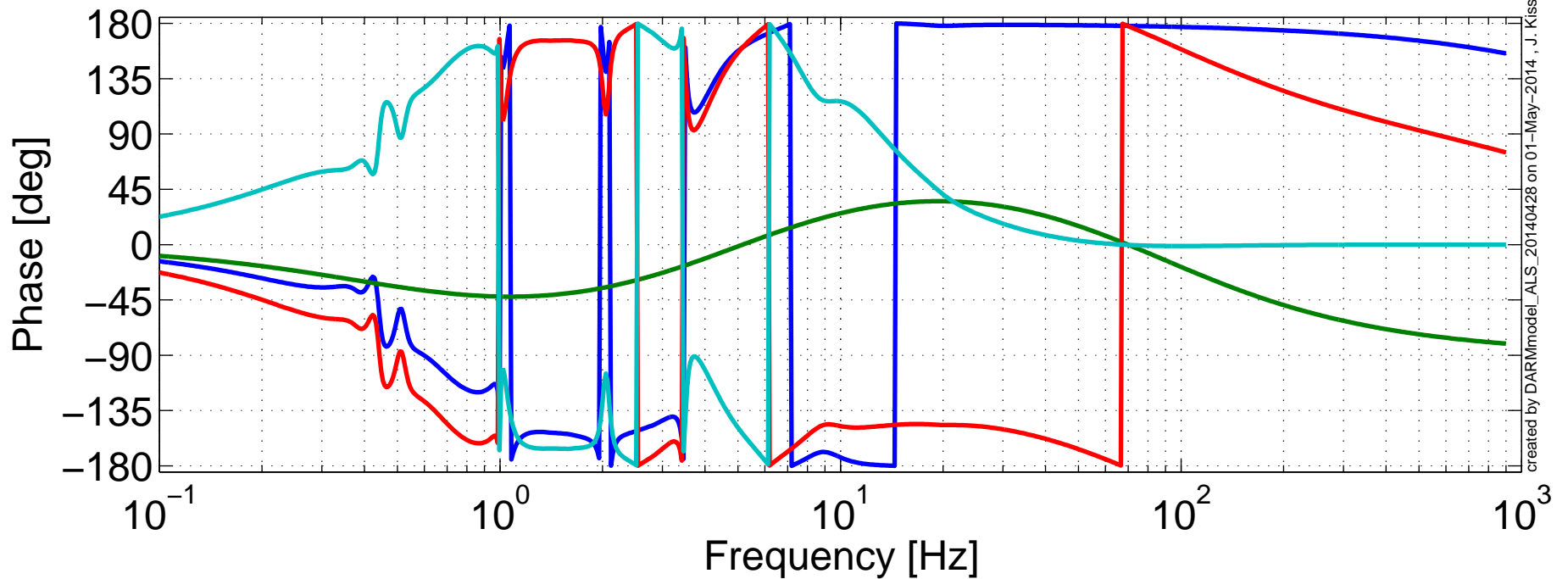
LUGF Phase Margins (red): [261 172] [deg]
 UUGF Phase Margins (blue): [30.1 32.1 36.6] [deg]



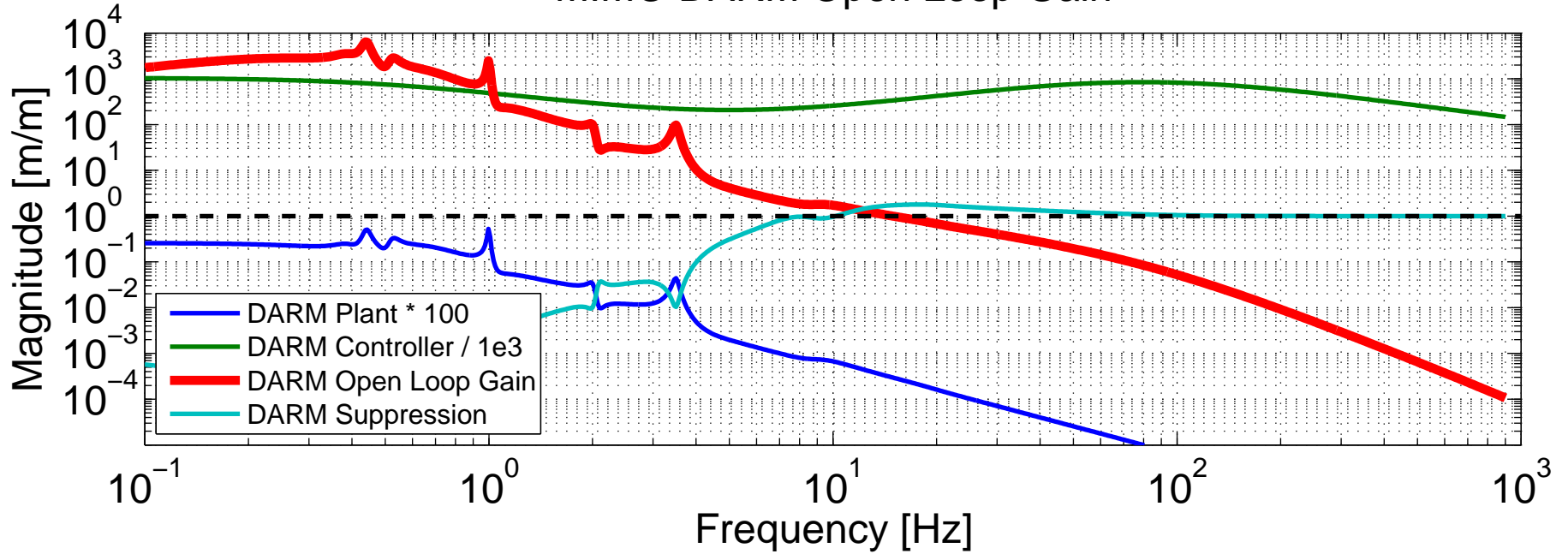
SISO DARM Open Loop Gain



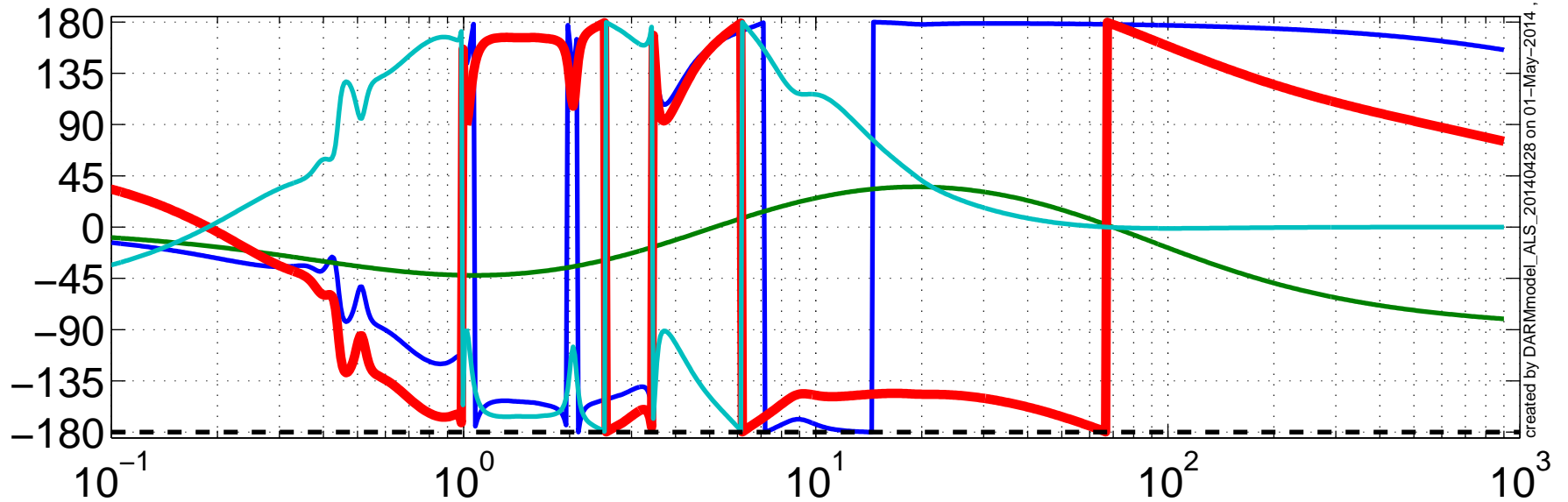
Phase Margin: 33.2428 @ 15 [Hz]



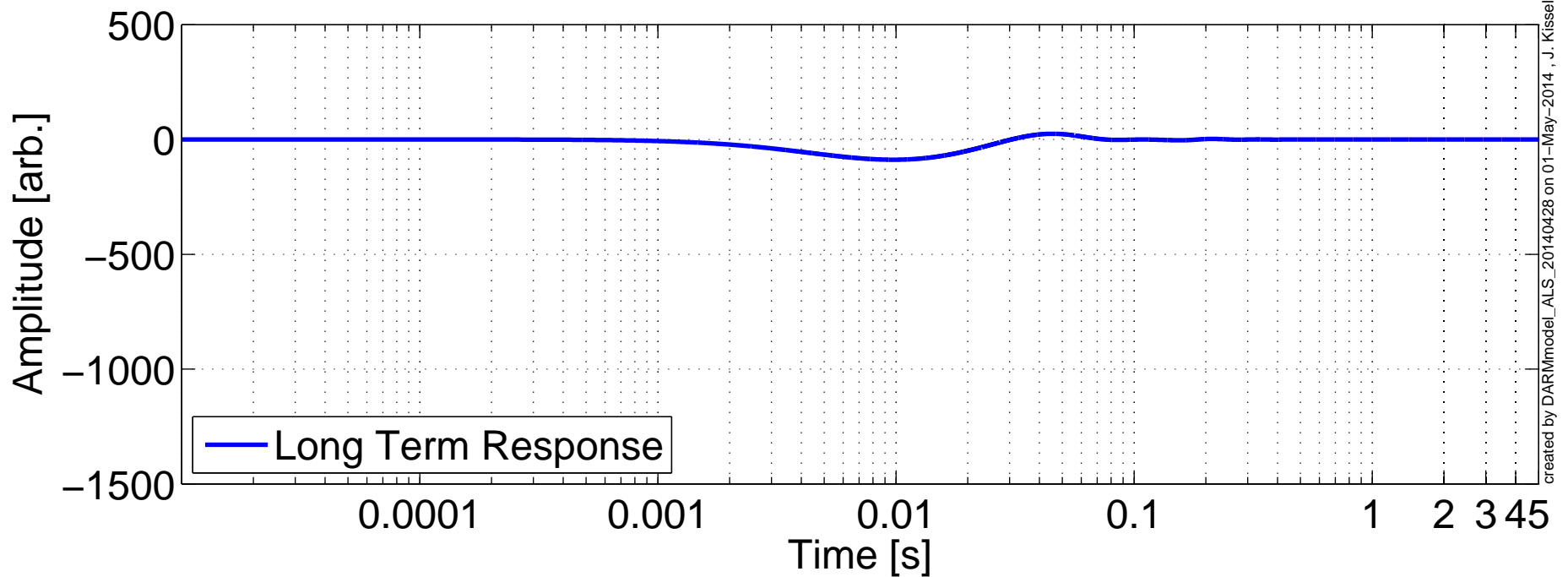
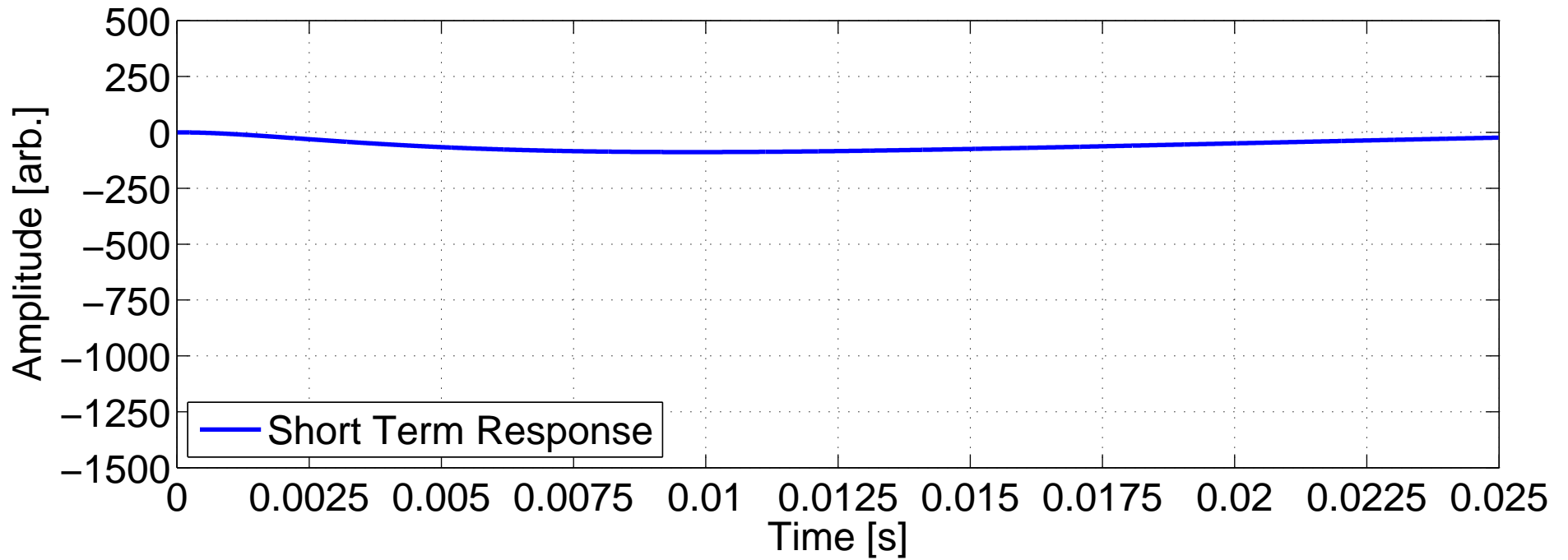
MIMO DARM Open Loop Gain



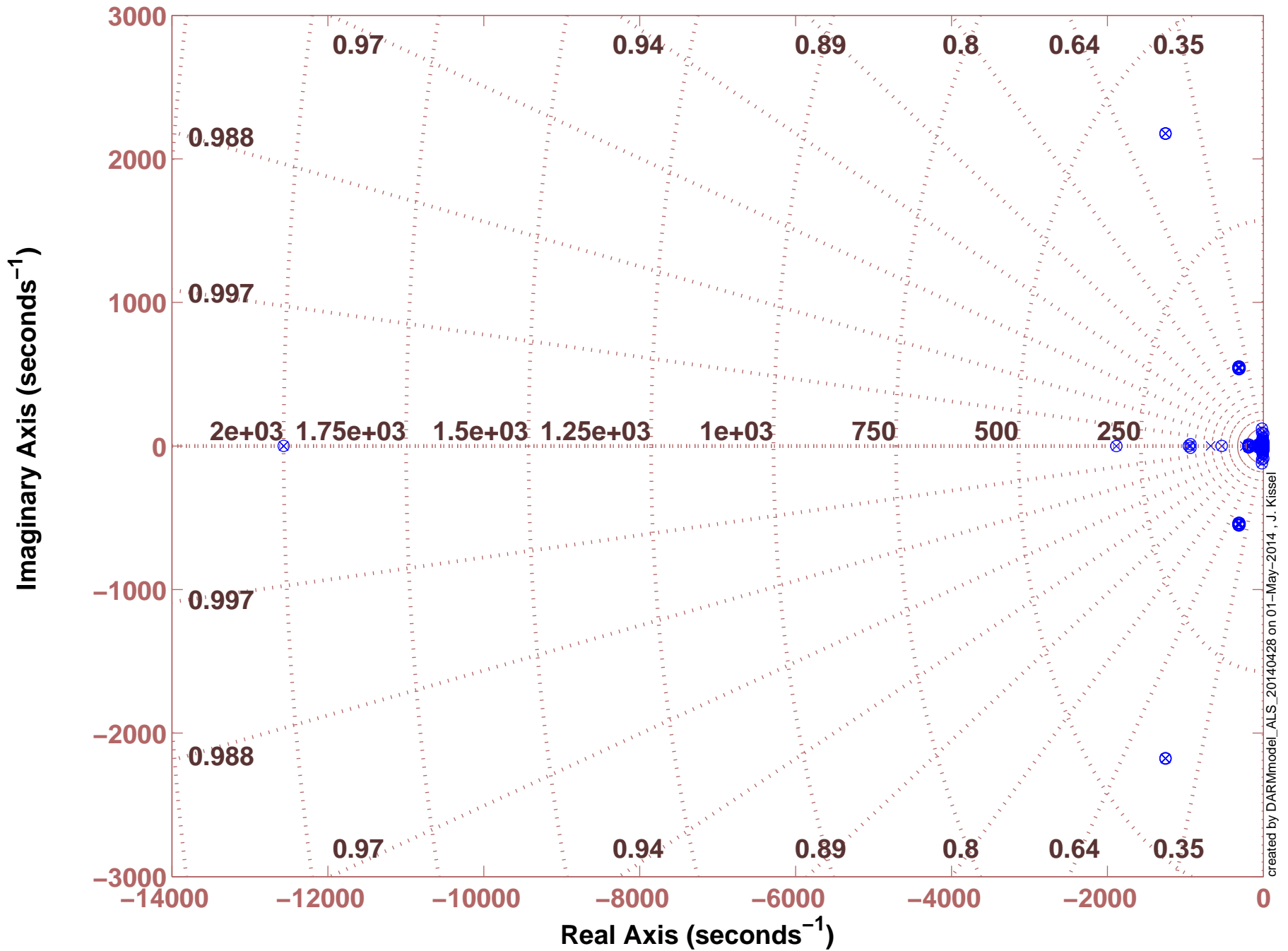
Max Gain Peaking: 1.79 @ 17.9 [Hz]
Phase Margin: 33.6 [deg] @ 15 [Hz]



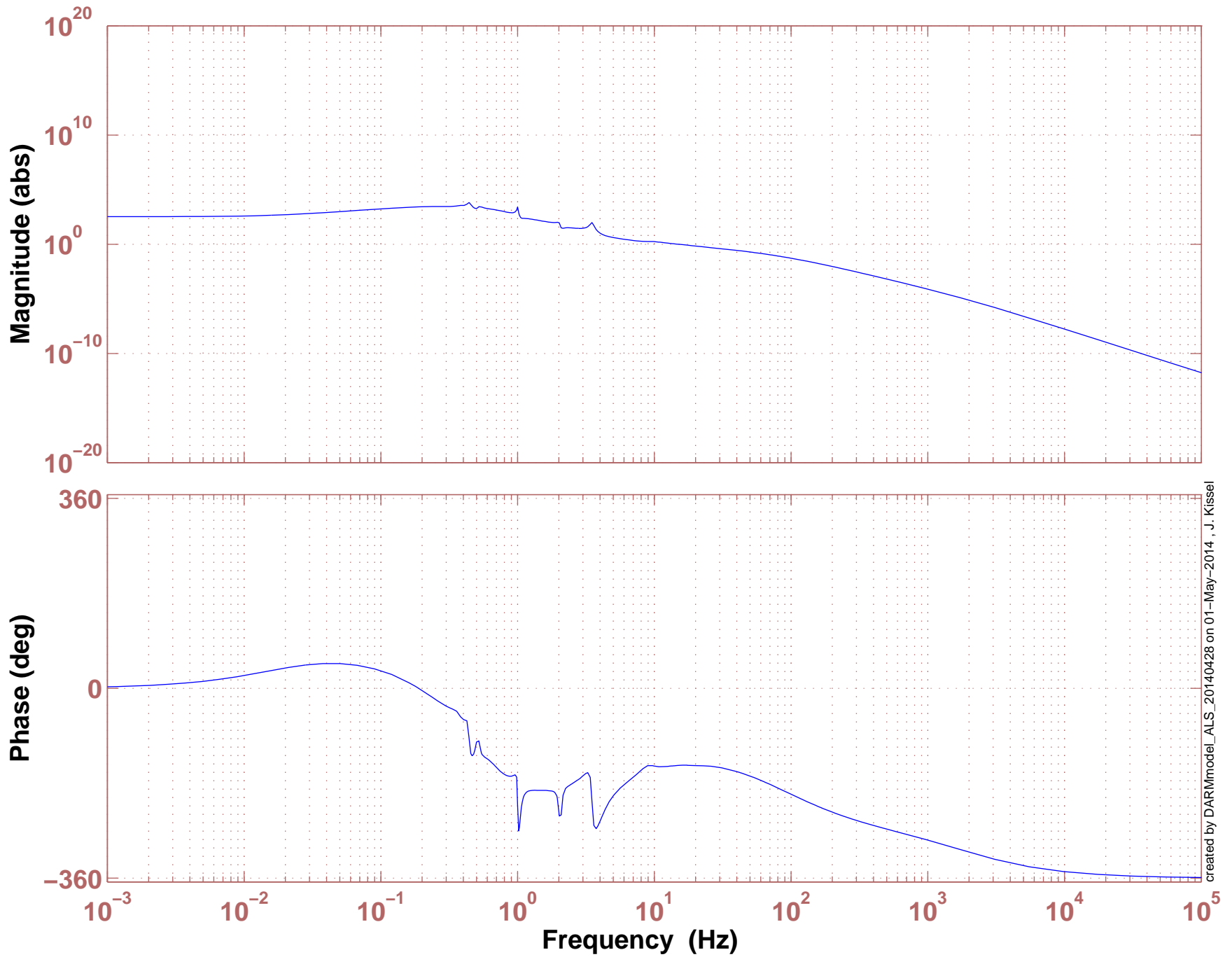
Impulse Response of Closed DARM Loop



Pole-Zero Map

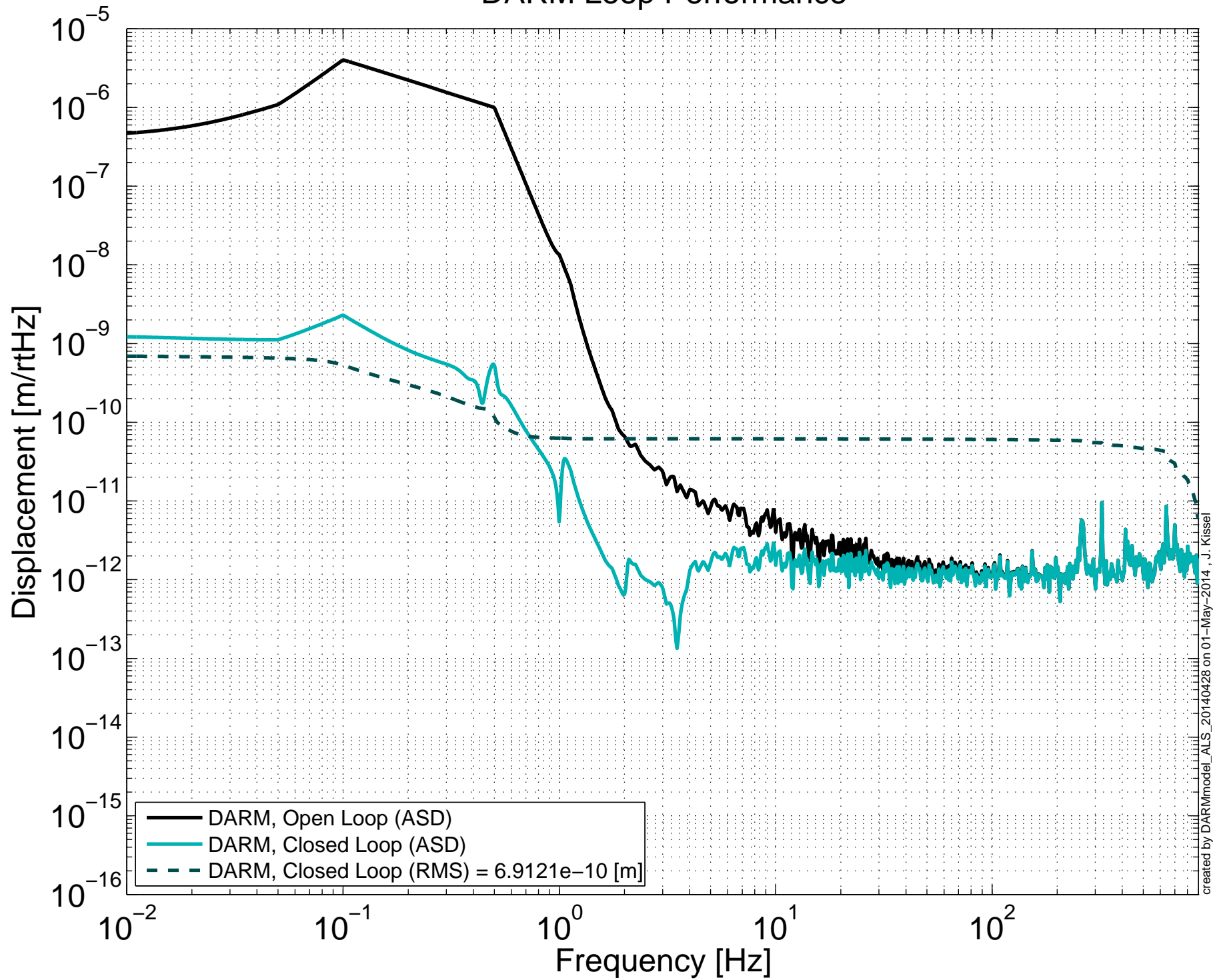


Bode Diagram



created by DARMmodel_ALS_20140428 on 01-May-2014, J. Kissel

DARM Loop Performance



Modeled DAC Voltage Desired vs. Available Control Force

