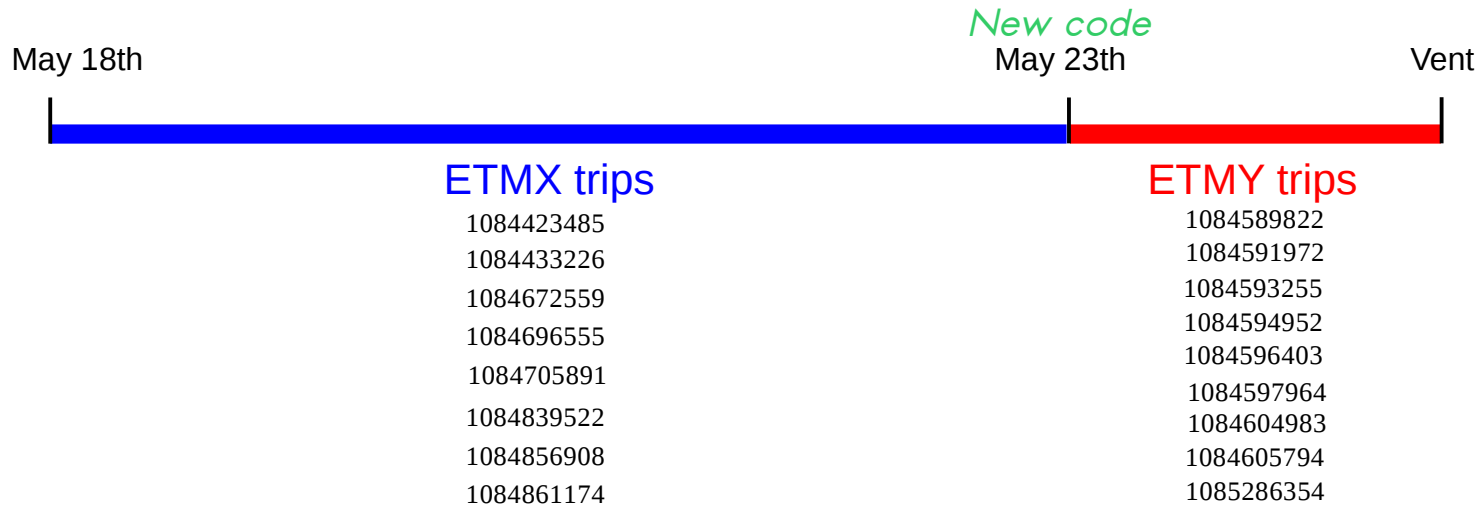


Lock loss at LHO

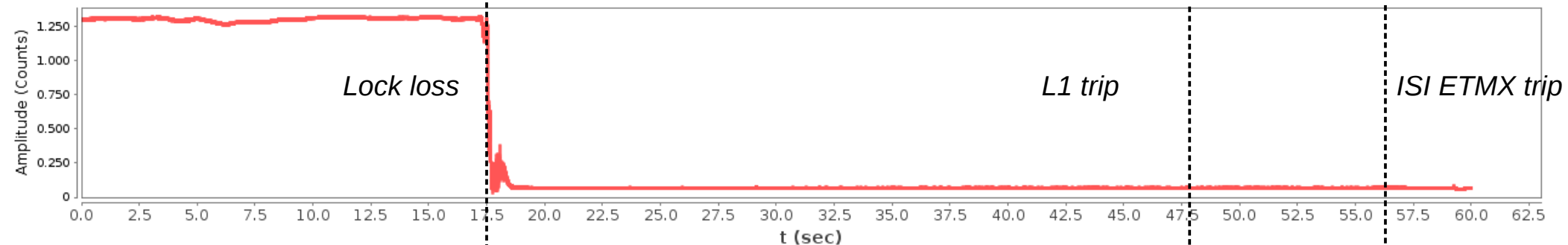
Trips due to lock loss → 2 distinct phases



All the ETMX trips present the same symptoms.
All the ETMY trips present the same symptoms.

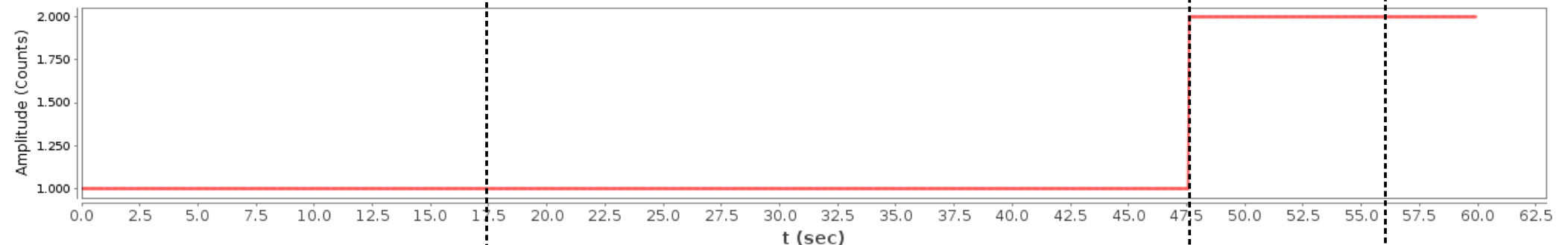
Starting with ETMX

**H1:ALS-C_TRX_A_LF_OUT_DQ t=60s at 2048Hz
2014-05-18 04:43:34 UTC (1084423430)**



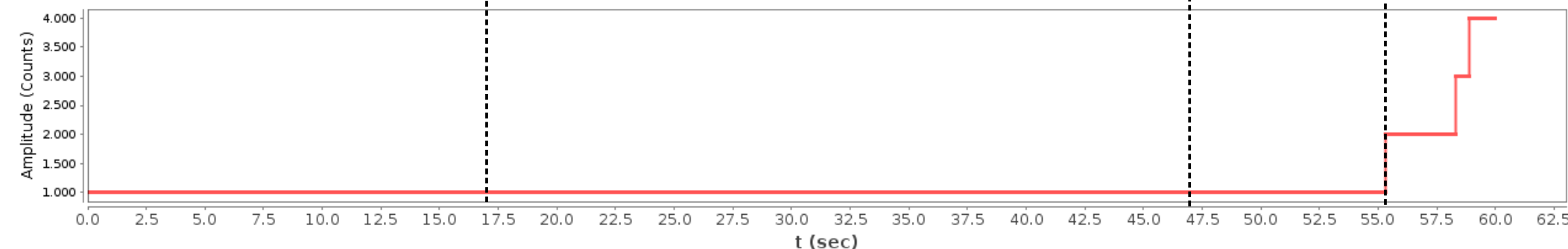
H1:ALS-C_TRX_A_LF_OUT_DQ t=60s at 2048Hz
2014-05-18 04:43:34 UTC (1084423430)

**H1:SUS-ETMX_L1_WDMON_STATE t=60s at 16Hz
2014-05-18 04:43:34 UTC (1084423430)**



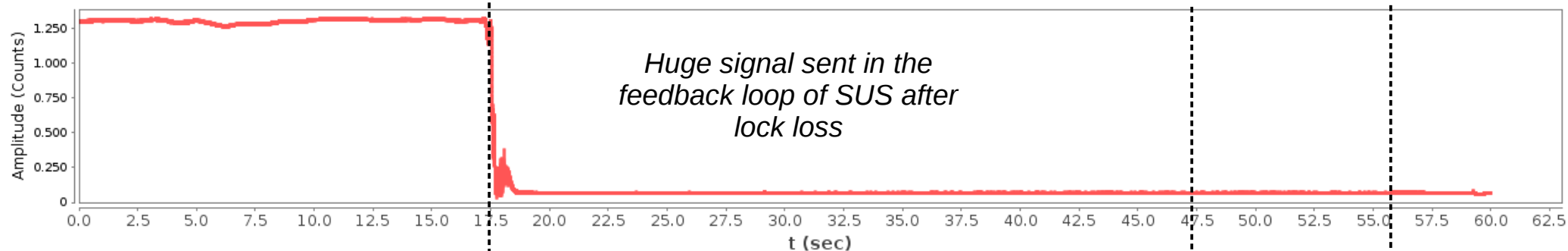
H1:SUS-ETMX_L1_WDMON_STATE t=60s at 16Hz
2014-05-18 04:43:34 UTC (1084423430)

**H1:ISI-ETMX_ST2_WD_MON_STATE_IN1_DQ t=60s at 4096Hz
2014-05-18 04:43:34 UTC (1084423430)**



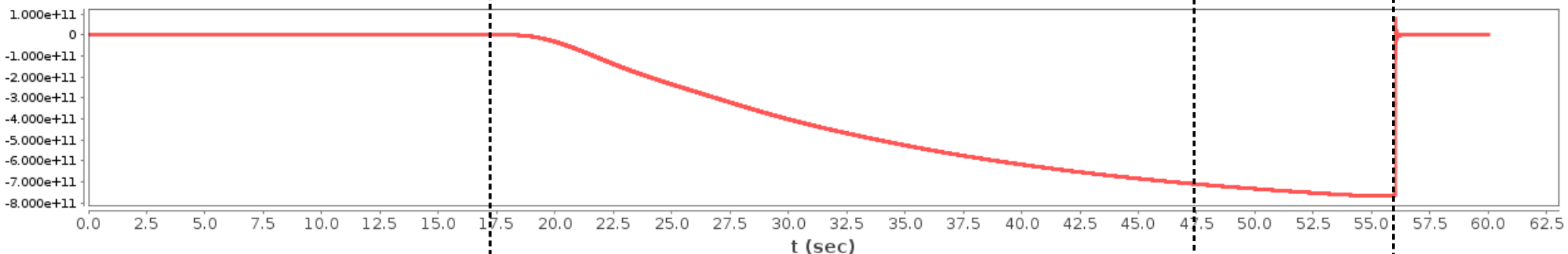
H1:ISI-ETMX_ST2_WD_MON_STATE_IN1_DQ t=60s at 4096Hz
2014-05-18 04:43:34 UTC (1084423430)

**H1:ALS-C_TRX_A_LF_OUT_DQ t=60s at 2048Hz
2014-05-18 04:43:34 UTC (1084423430)**



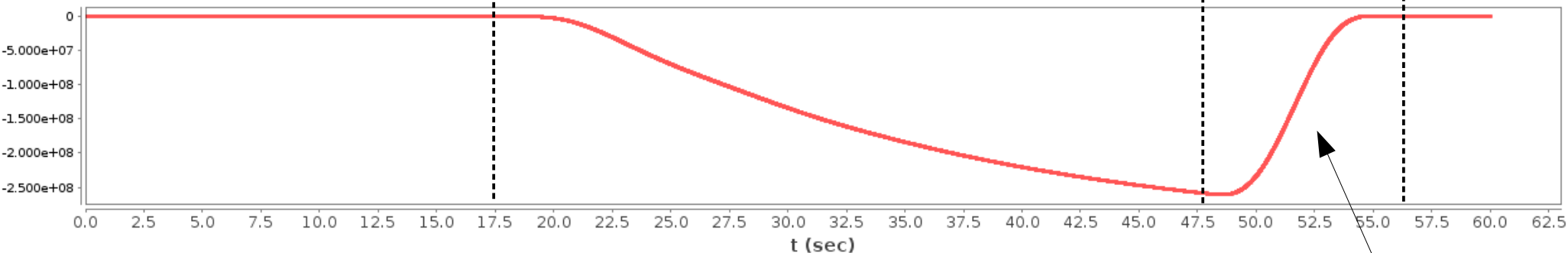
H1:ALS-C_TRX_A_LF_OUT_DQ t=60s at 2048Hz
2014-05-18 04:43:34 UTC (1084423430)

**H1:LSC-DARM_CTRL_256_DQ t=60s at 256Hz
2014-05-18 04:43:34 UTC (1084423430)**



H1:LSC-DARM_CTRL_256_DQ t=60s at 256Hz
2014-05-18 04:43:34 UTC (1084423430)

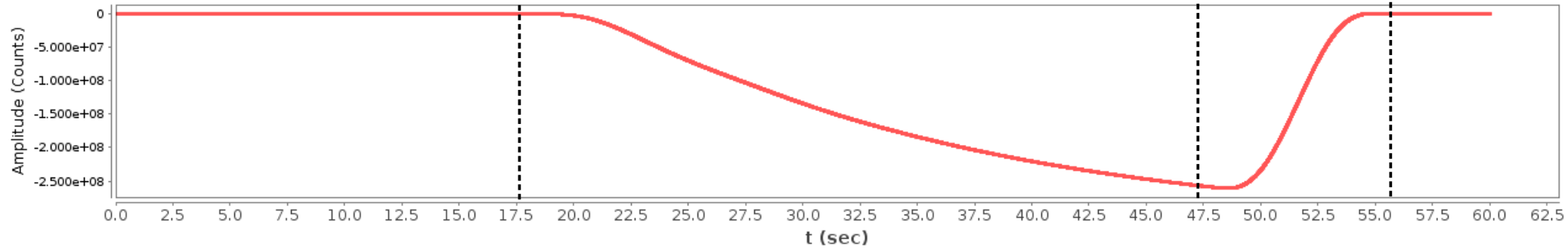
**H1:SUS-ETMX_M0_LOCK_L_OUT_DQ t=60s at 512Hz
2014-05-18 04:43:34 UTC (1084423430)**



H1:SUS-ETMX_M0_LOCK_L_OUT_DQ t=60s at 512Hz
2014-05-18 04:43:34 UTC (1084423430)

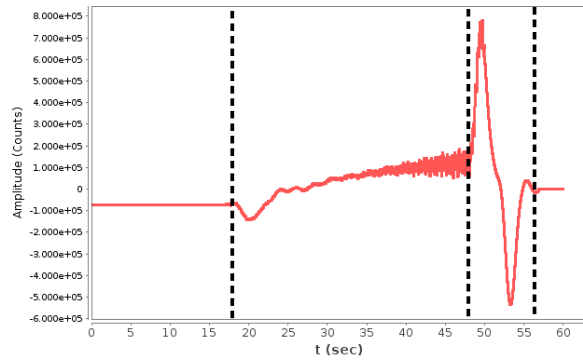
SUS guardian

H1:SUS-ETMX_M0_LOCK_L_OUT_DQ t=60s at 512Hz 2014-05-18 04:43:34 UTC (1084423430)



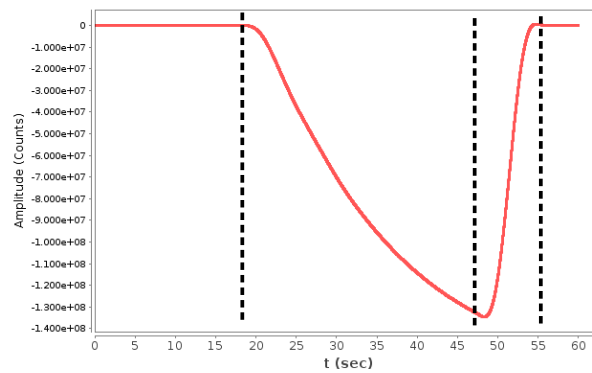
H1:SUS-ETMX_M0_LOCK_L_OUT_DQ t=60s at 512Hz
2014-05-18 04:43:34 UTC (1084423430)

H1:SUS-ETMX_M0_MASTER_OUT_F1_DQ t=60s at 512Hz 2014-05-18 04:43:34 UTC (1084423430)



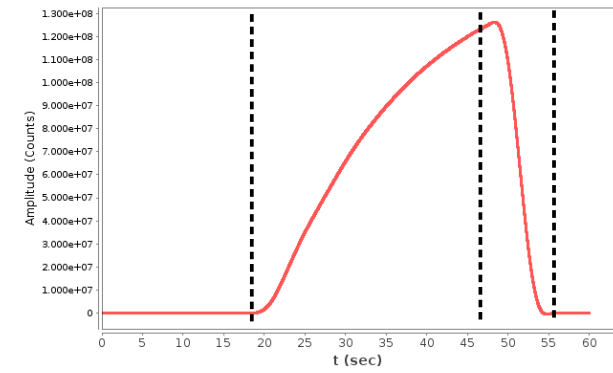
H1:SUS-ETMX_M0_MASTER_OUT_F1_DQ t=60s at 512Hz
2014-05-18 04:43:34 UTC (1084423430)

H1:SUS-ETMX_M0_MASTER_OUT_F2_DQ t=60s at 512Hz 2014-05-18 04:43:34 UTC (1084423430)



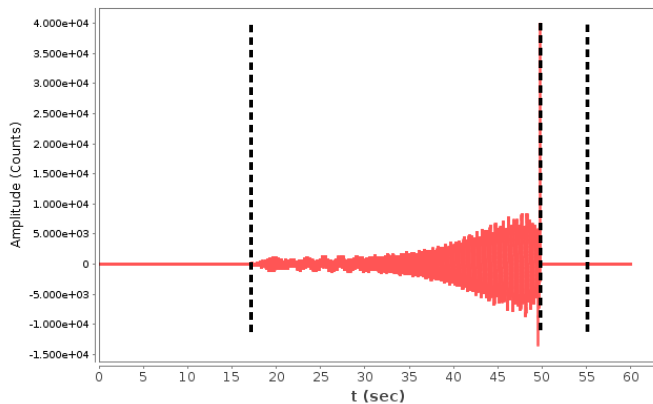
H1:SUS-ETMX_M0_MASTER_OUT_F2_DQ t=60s at 512Hz
2014-05-18 04:43:34 UTC (1084423430)

H1:SUS-ETMX_M0_MASTER_OUT_F3_DQ t=60s at 512Hz 2014-05-18 04:43:34 UTC (1084423430)



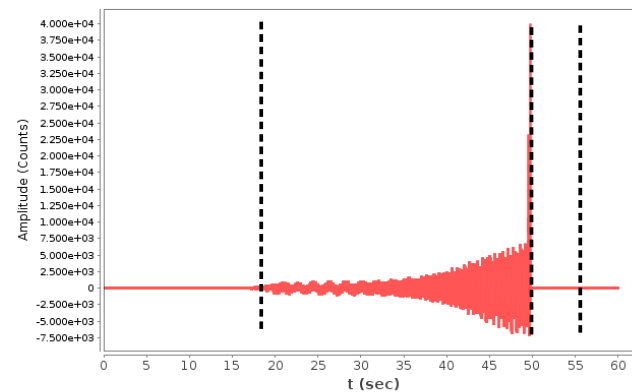
H1:SUS-ETMX_M0_MASTER_OUT_F3_DQ t=60s at 512Hz
2014-05-18 04:43:34 UTC (1084423430)

H1:SUS-ETMX_M0_MASTER_OUT_LF_DQ t=60s at 512Hz 2014-05-18 04:43:34 UTC (1084423430)



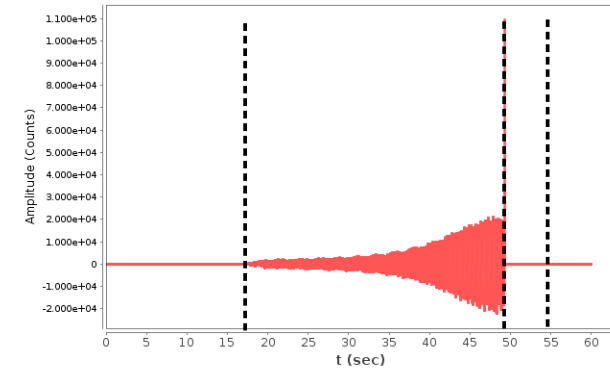
H1:SUS-ETMX_M0_MASTER_OUT_LF_DQ t=60s at 512Hz
2014-05-18 04:43:34 UTC (1084423430)

H1:SUS-ETMX_M0_MASTER_OUT_RT_DQ t=60s at 512Hz 2014-05-18 04:43:34 UTC (1084423430)



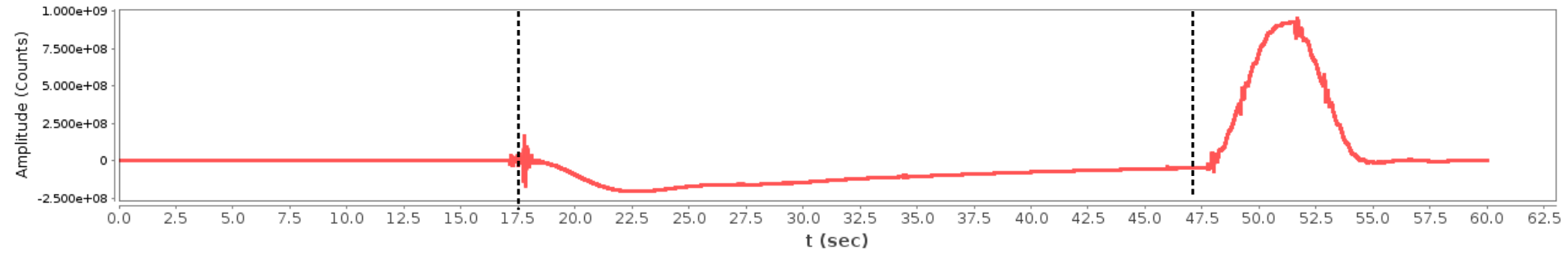
H1:SUS-ETMX_M0_MASTER_OUT_RT_DQ t=60s at 512Hz
2014-05-18 04:43:34 UTC (1084423430)

H1:SUS-ETMX_M0_MASTER_OUT_SD_DQ t=60s at 512Hz 2014-05-18 04:43:34 UTC (1084423430)



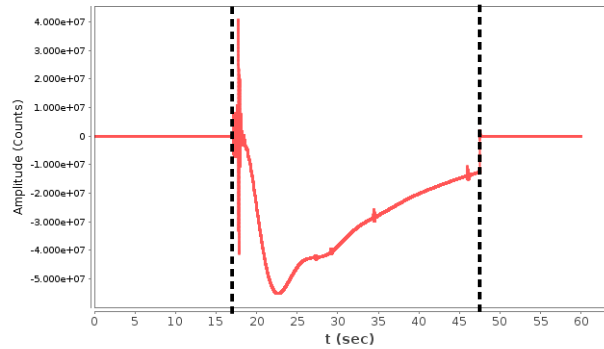
H1:SUS-ETMX_M0_MASTER_OUT_SD_DQ t=60s at 512Hz
2014-05-18 04:43:34 UTC (1084423430)

H1:SUS-ETMX_L1_LOCK_L_OUT_DQ t=60s at 1024Hz 2014-05-18 04:43:34 UTC (1084423430)



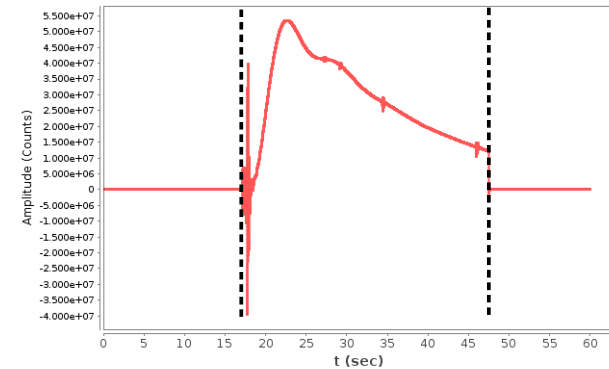
H1:SUS-ETMX_L1_LOCK_L_OUT_DQ t=60s at 1024Hz
2014-05-18 04:43:34 UTC (1084423430)

H1:SUS-ETMX_L1_MASTER_OUT_UR_DQ t=60s at 1024Hz 2014-05-18 04:43:34 UTC (1084423430)



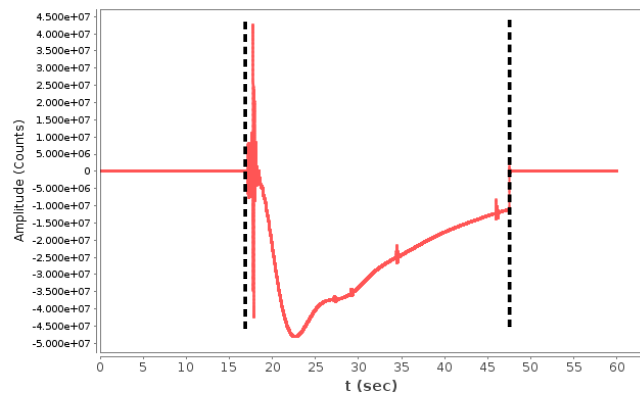
H1:SUS-ETMX_L1_MASTER_OUT_UR_DQ t=60s at 1024Hz
2014-05-18 04:43:34 UTC (1084423430)

H1:SUS-ETMX_L1_MASTER_OUT_UL_DQ t=60s at 1024Hz 2014-05-18 04:43:34 UTC (1084423430)



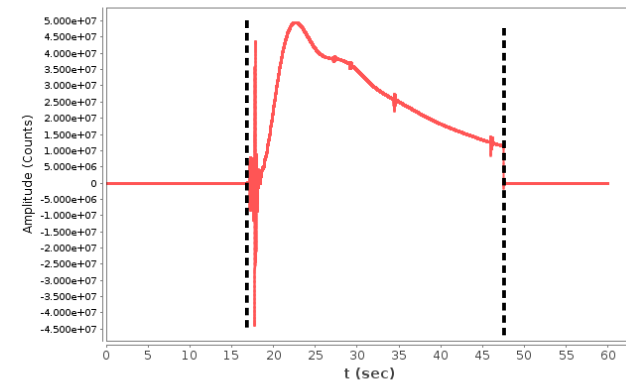
H1:SUS-ETMX_L1_MASTER_OUT_UL_DQ t=60s at 1024Hz
2014-05-18 04:43:34 UTC (1084423430)

H1:SUS-ETMX_L1_MASTER_OUT_LL_DQ t=60s at 1024Hz 2014-05-18 04:43:34 UTC (1084423430)



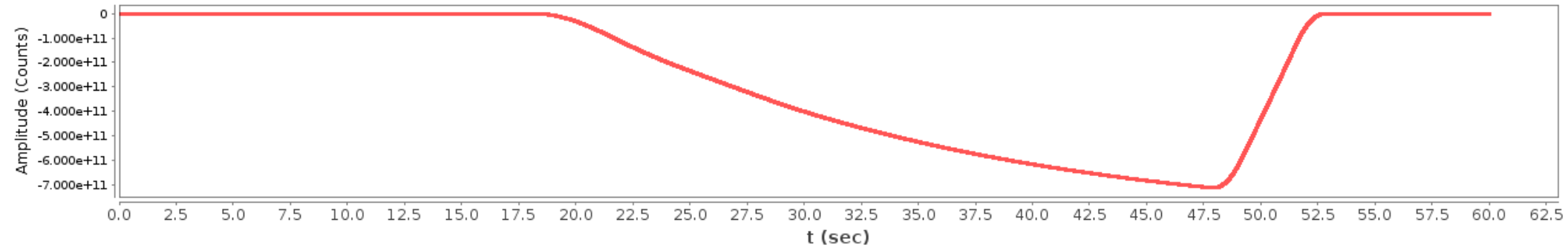
H1:SUS-ETMX_L1_MASTER_OUT_LL_DQ t=60s at 1024Hz
2014-05-18 04:43:34 UTC (1084423430)

H1:SUS-ETMX_L1_MASTER_OUT_LR_DQ t=60s at 1024Hz 2014-05-18 04:43:34 UTC (1084423430)



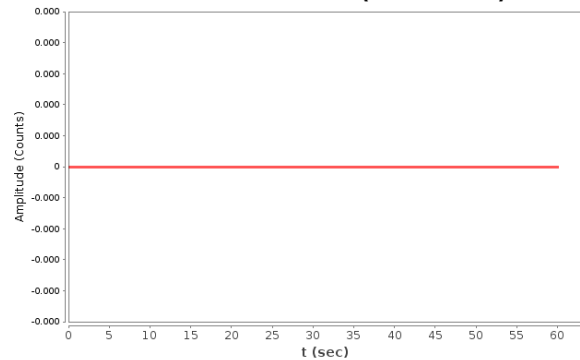
H1:SUS-ETMX_L1_MASTER_OUT_LR_DQ t=60s at 1024Hz
2014-05-18 04:43:34 UTC (1084423430)

H1:SUS-ETMX_L2_LOCK_L_OUT_DQ t=60s at 2048Hz 2014-05-18 04:43:34 UTC (1084423430)



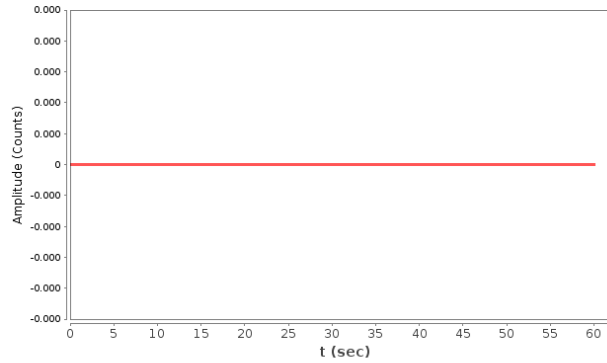
H1:SUS-ETMX_L2_LOCK_L_OUT_DQ t=60s at 2048Hz
2014-05-18 04:43:34 UTC (1084423430)

H1:SUS-ETMX_L2_MASTER_OUT_UL_DQ t=60s at 2048Hz 2014-05-18 04:43:34 UTC (1084423430)



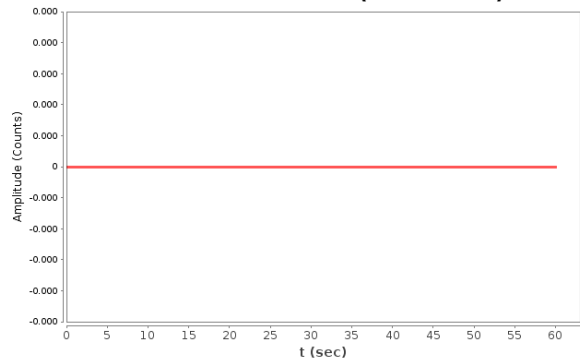
H1:SUS-ETMX_L2_MASTER_OUT_UL_DQ t=60s at 2048Hz
2014-05-18 04:43:34 UTC (1084423430)

H1:SUS-ETMX_L2_MASTER_OUT_UR_DQ t=60s at 2048Hz 2014-05-18 04:43:34 UTC (1084423430)



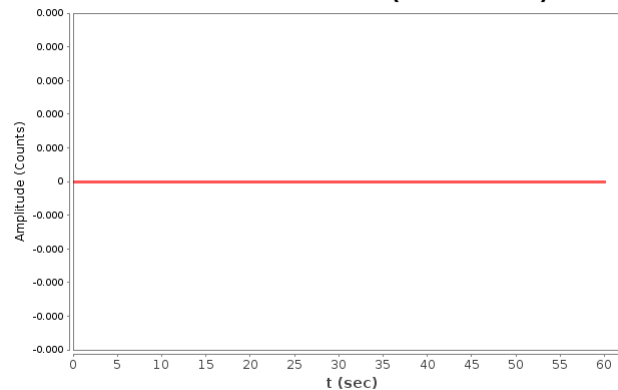
H1:SUS-ETMX_L2_MASTER_OUT_UR_DQ t=60s at 2048Hz
2014-05-18 04:43:34 UTC (1084423430)

H1:SUS-ETMX_L2_MASTER_OUT_LL_DQ t=60s at 2048Hz 2014-05-18 04:43:34 UTC (1084423430)



H1:SUS-ETMX_L2_MASTER_OUT_LL_DQ t=60s at 2048Hz
2014-05-18 04:43:34 UTC (1084423430)

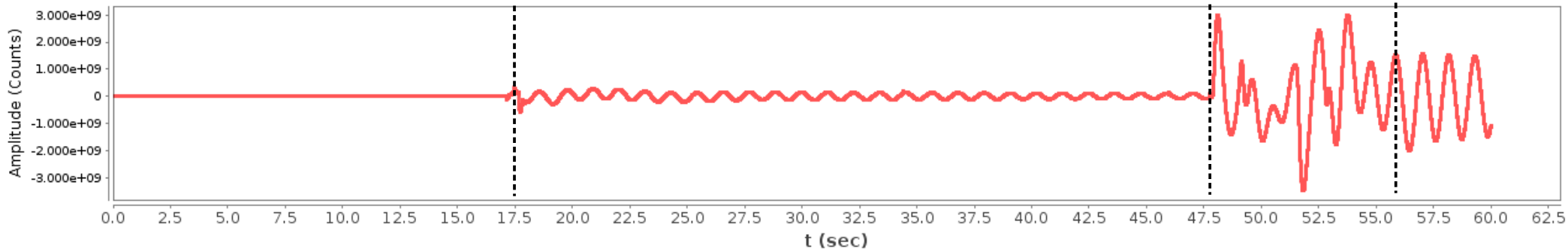
H1:SUS-ETMX_L2_MASTER_OUT_LR_DQ t=60s at 2048Hz 2014-05-18 04:43:34 UTC (1084423430)



H1:SUS-ETMX_L2_MASTER_OUT_LR_DQ t=60s at 2048Hz
2014-05-18 04:43:34 UTC (1084423430)

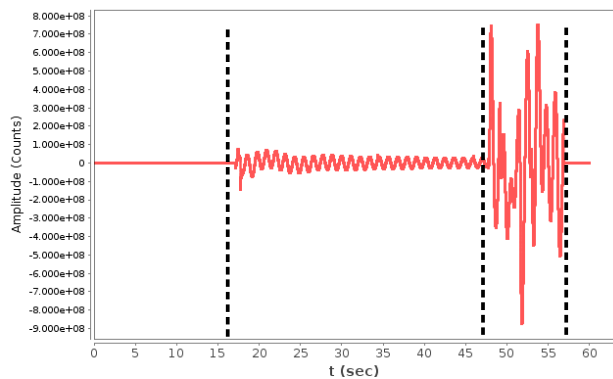
Nothing sent on L2

H1:SUS-ETMX_L3_LOCK_L_OUT_DQ t=60s at 2048Hz 2014-05-18 04:43:34 UTC (1084423430)



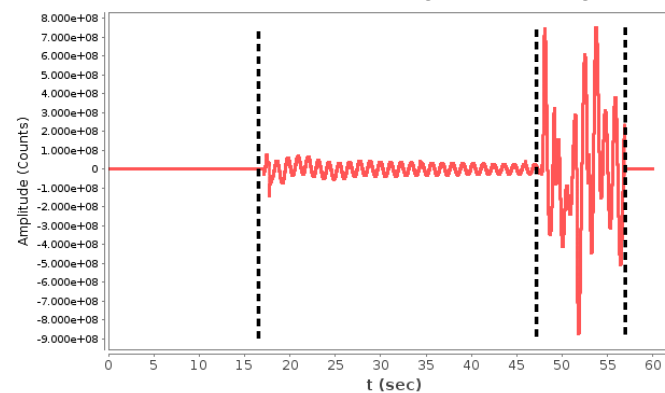
H1:SUS-ETMX_L3_LOCK_L_OUT_DQ t=60s at 2048Hz
2014-05-18 04:43:34 UTC (1084423430)

H1:SUS-ETMX_L3_MASTER_OUT_UL_DQ t=60s at 2048Hz 2014-05-18 04:43:34 UTC (1084423430)



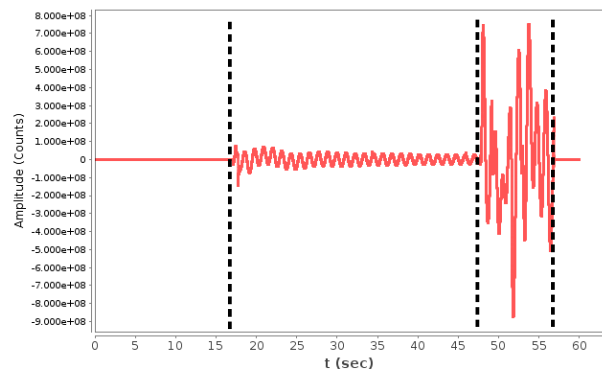
H1:SUS-ETMX_L3_MASTER_OUT_UL_DQ t=60s at 2048Hz
2014-05-18 04:43:34 UTC (1084423430)

H1:SUS-ETMX_L3_MASTER_OUT_UR_DQ t=60s at 2048Hz 2014-05-18 04:43:34 UTC (1084423430)



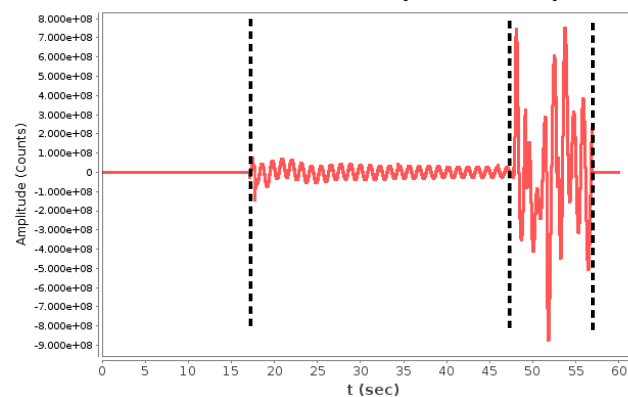
H1:SUS-ETMX_L3_MASTER_OUT_UR_DQ t=60s at 2048Hz
2014-05-18 04:43:34 UTC (1084423430)

H1:SUS-ETMX_L3_MASTER_OUT_LL_DQ t=60s at 2048Hz 2014-05-18 04:43:34 UTC (1084423430)



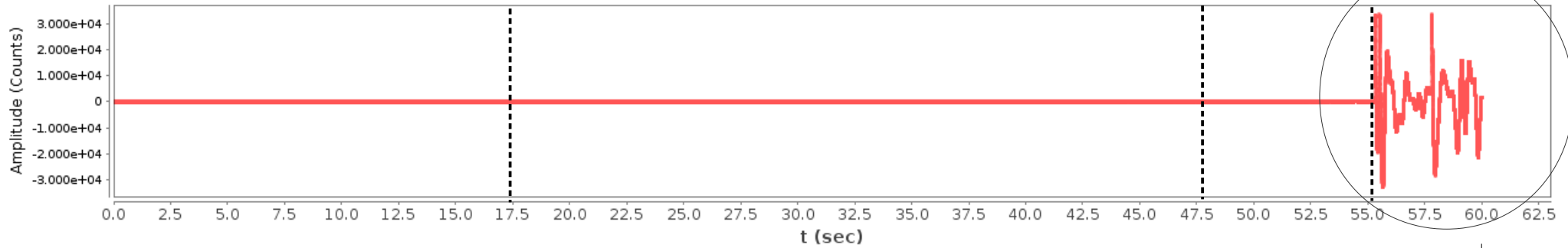
H1:SUS-ETMX_L3_MASTER_OUT_LL_DQ t=60s at 2048Hz
2014-05-18 04:43:34 UTC (1084423430)

H1:SUS-ETMX_L3_MASTER_OUT_LR_DQ t=60s at 2048Hz 2014-05-18 04:43:34 UTC (1084423430)

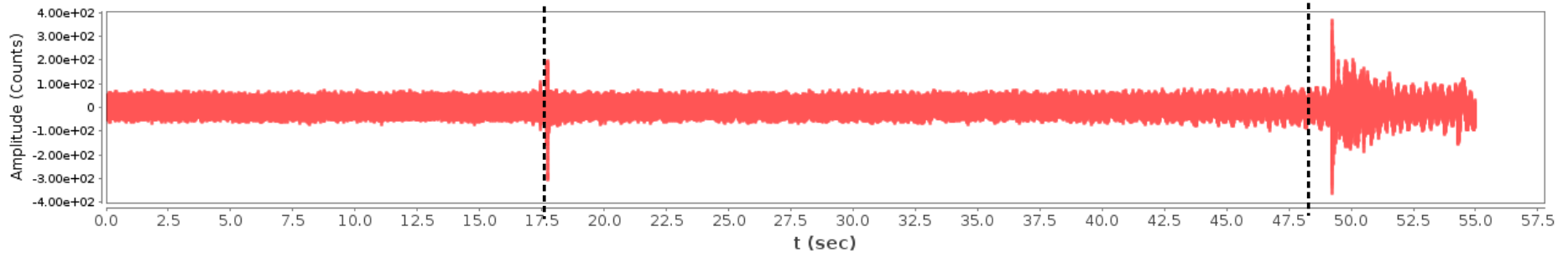


H1:SUS-ETMX_L3_MASTER_OUT_LR_DQ t=60s at 2048Hz
2014-05-18 04:43:34 UTC (1084423430)

**H1:ISI-ETMX_ST2_GS13INF_V1_IN1_DQ t=60s at 4096Hz
2014-05-18 04:43:34 UTC (1084423430)**

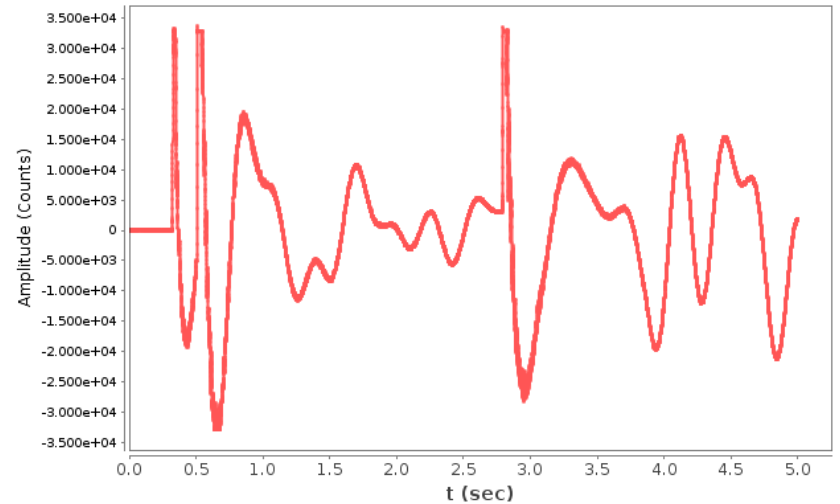


**H1:ISI-ETMX_ST2_GS13INF_V1_IN1_DQ t=55s at 4096Hz
2014-05-18 04:43:34 UTC (1084423430)**



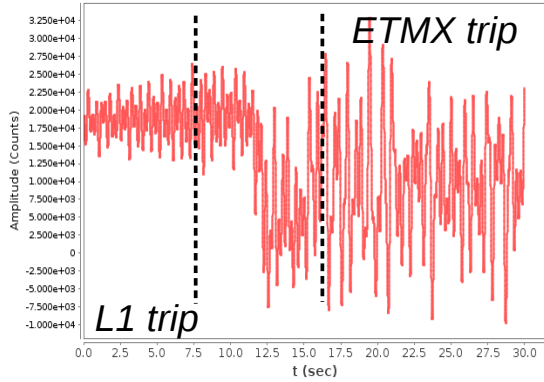
H1:ISI-ETMX_ST2_GS13INF_V1_IN1_DQ t=55s at 4096Hz
2014-05-18 04:43:34 UTC (1084423430)

**H1:ISI-ETMX_ST2_GS13INF_V1_IN1_DQ t=5s at 4096Hz
2014-05-18 04:44:29 UTC (1084423485)**



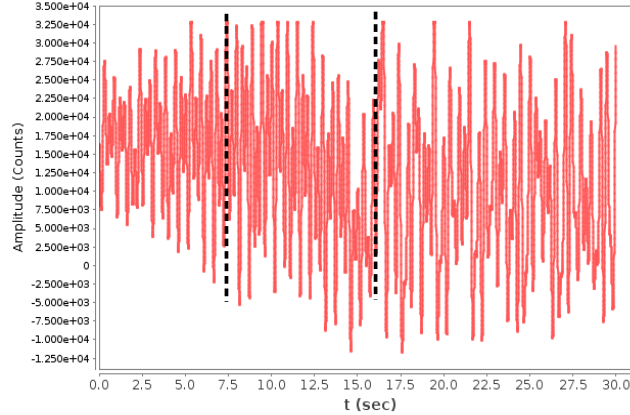
H1:ISI-ETMX_ST2_GS13INF_V1_IN1_DQ t=5s at 4096Hz
2014-05-18 04:44:29 UTC (1084423485)

H1:SUS-ETMX_M0_OSEMINF_F1_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)



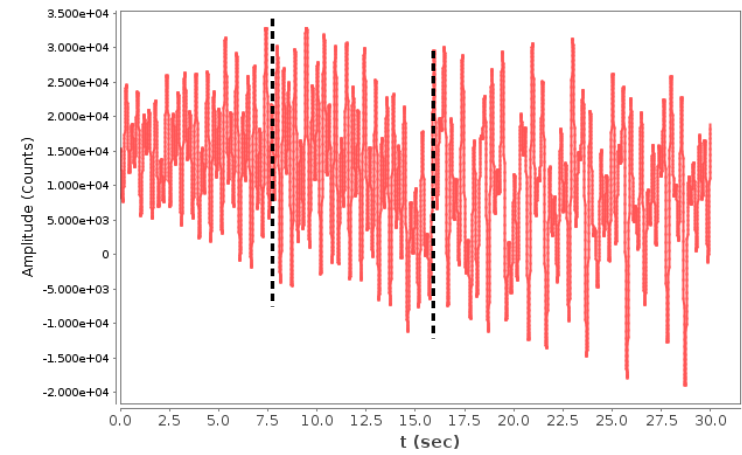
H1:SUS-ETMX_M0_OSEMINF_F1_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)

H1:SUS-ETMX_M0_OSEMINF_F2_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)



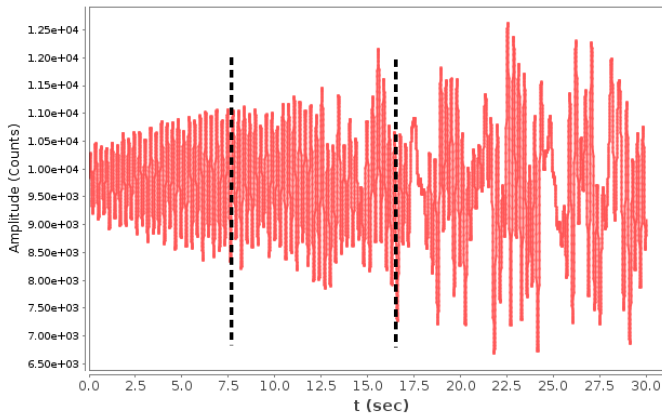
H1:SUS-ETMX_M0_OSEMINF_F2_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)

H1:SUS-ETMX_M0_OSEMINF_F3_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)



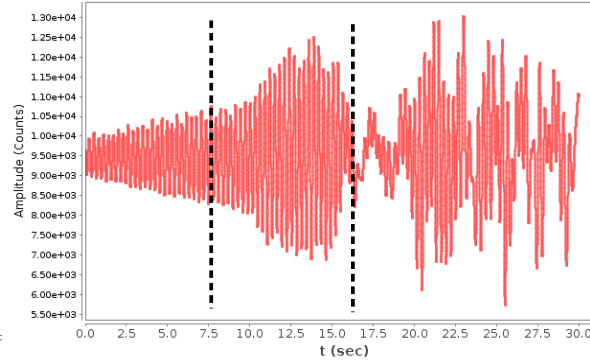
H1:SUS-ETMX_M0_OSEMINF_F3_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)

H1:SUS-ETMX_M0_OSEMINF_LF_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)



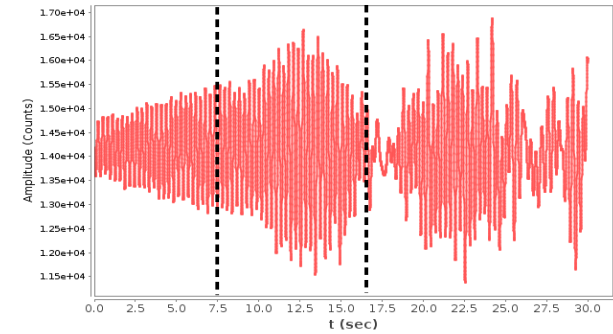
H1:SUS-ETMX_M0_OSEMINF_LF_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)

H1:SUS-ETMX_M0_OSEMINF_RT_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)



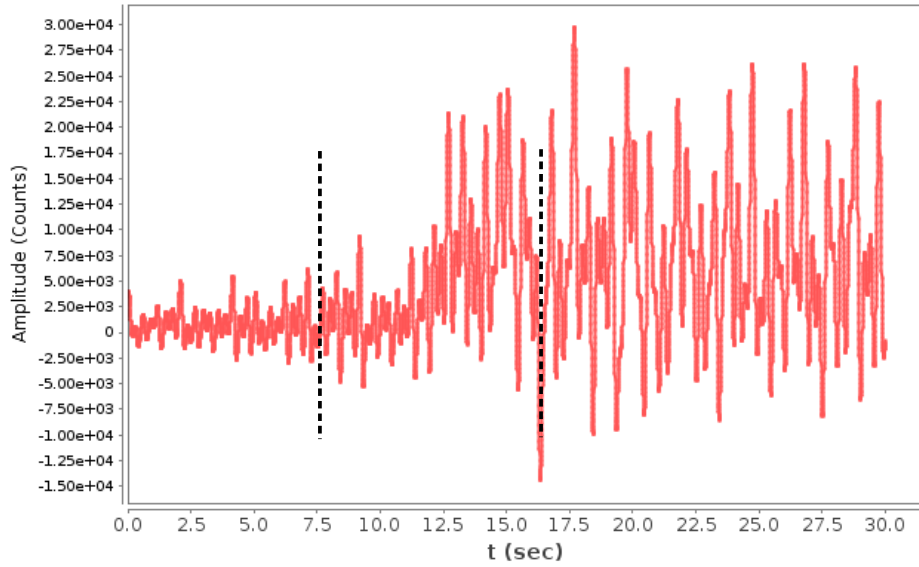
H1:SUS-ETMX_M0_OSEMINF_RT_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)

H1:SUS-ETMX_M0_OSEMINF_SD_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)



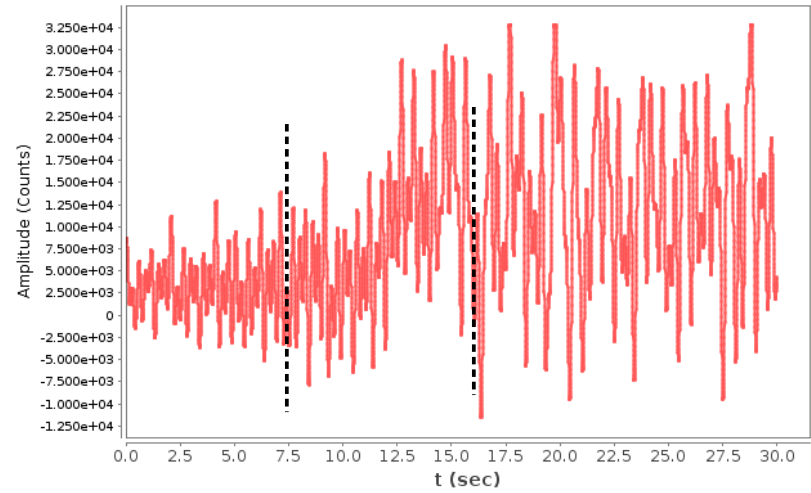
H1:SUS-ETMX_M0_OSEMINF_SD_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)

H1:SUS-ETMX_L1_OSEMINF_UL_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)



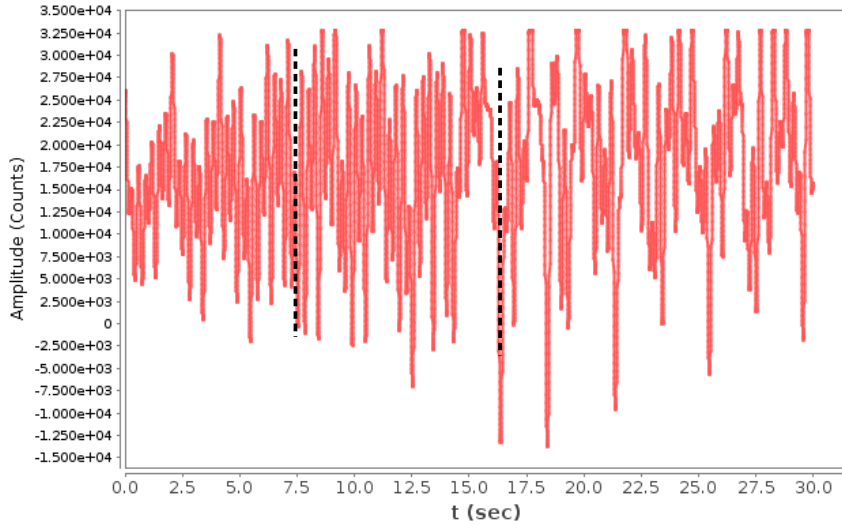
H1:SUS-ETMX_L1_OSEMINF_UL_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)

H1:SUS-ETMX_L1_OSEMINF_UR_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)



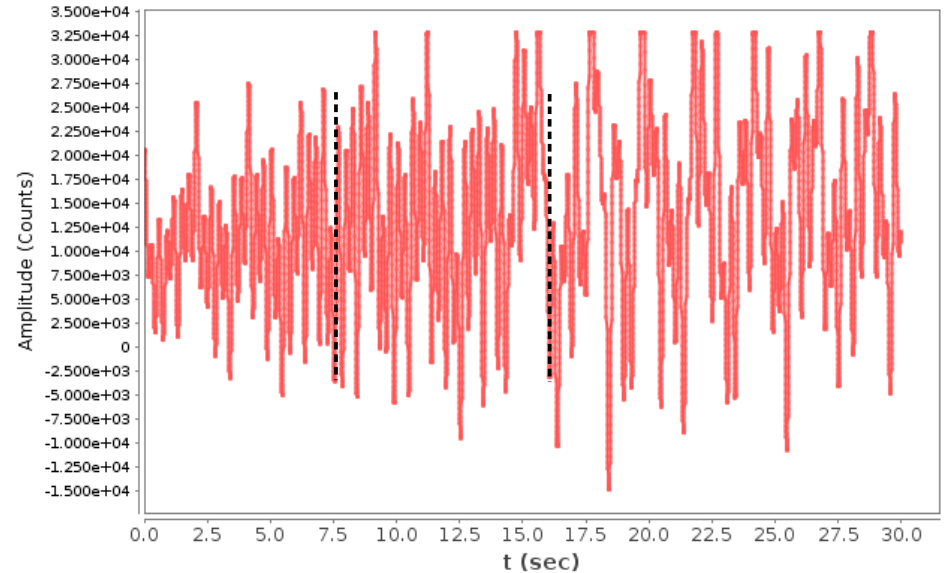
H1:SUS-ETMX_L1_OSEMINF_UR_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)

H1:SUS-ETMX_L1_OSEMINF_LL_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)



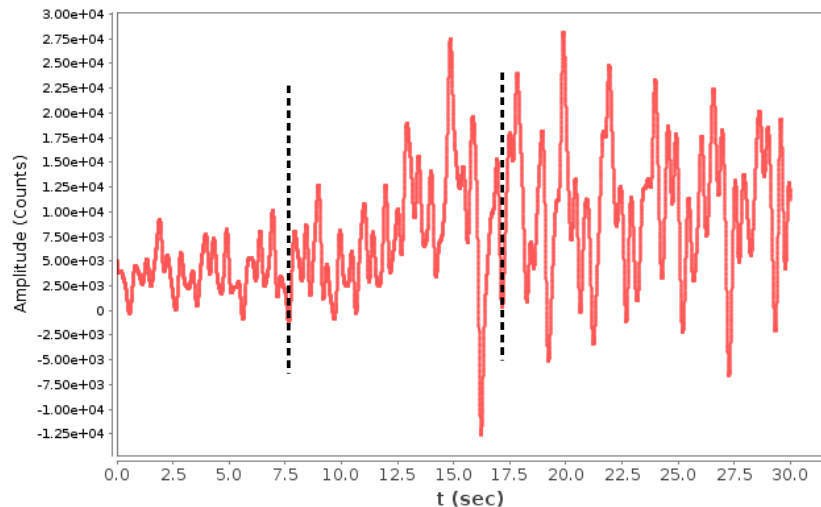
H1:SUS-ETMX_L1_OSEMINF_LL_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)

H1:SUS-ETMX_L1_OSEMINF_LR_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)



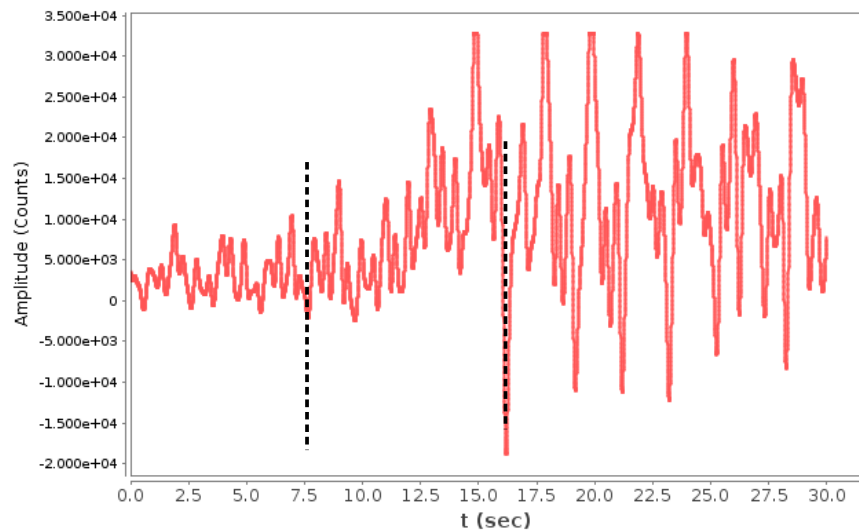
H1:SUS-ETMX_L1_OSEMINF_LR_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)

H1:SUS-ETMX_L2_OSEMINF_UL_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)



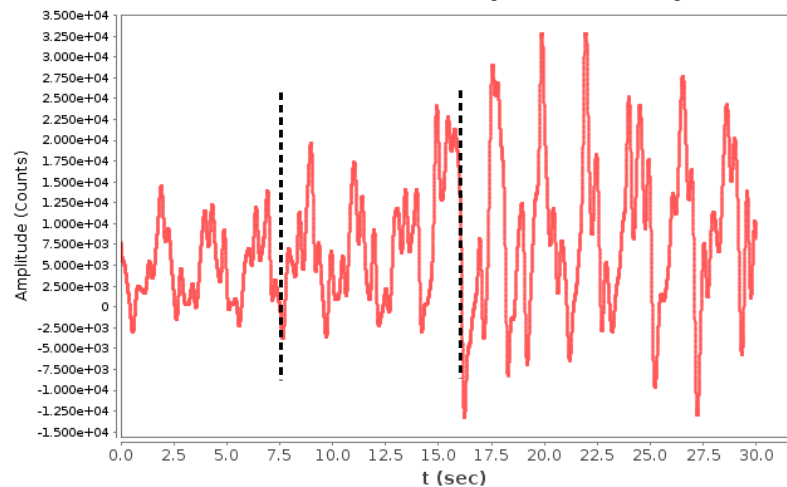
H1:SUS-ETMX_L2_OSEMINF_UL_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)

H1:SUS-ETMX_L2_OSEMINF_UR_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)



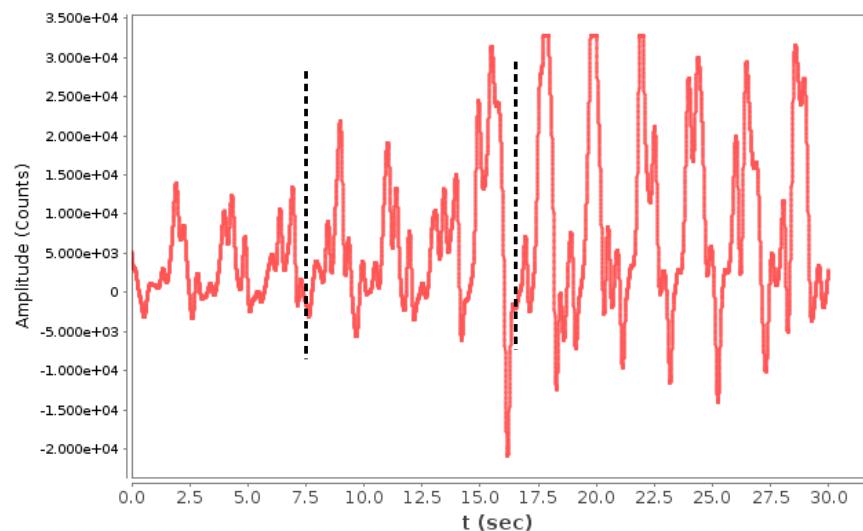
H1:SUS-ETMX_L2_OSEMINF_UR_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)

H1:SUS-ETMX_L2_OSEMINF_LL_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)



H1:SUS-ETMX_L2_OSEMINF_LL_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)

H1:SUS-ETMX_L2_OSEMINF_LR_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)

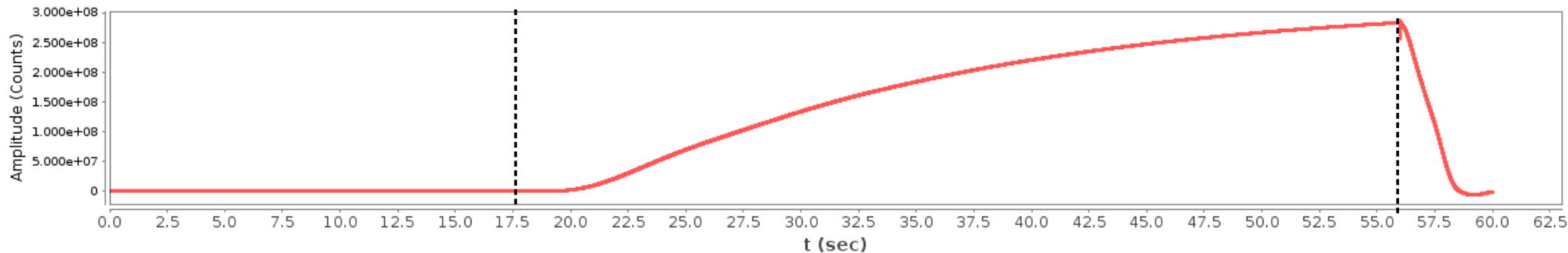


H1:SUS-ETMX_L2_OSEMINF_LR_IN1_DQ t=30s at 256Hz
2014-05-18 04:44:14 UTC (1084423470)

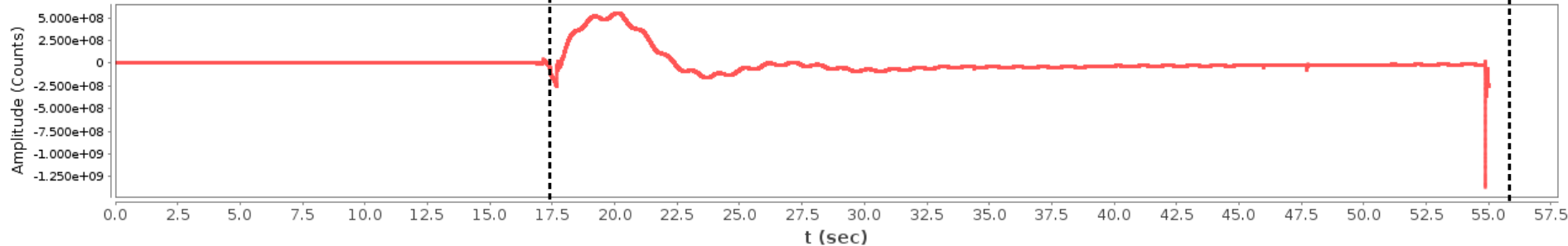
Same behavior on ETMY (without the L1/ISI trip)

H1:SUS-ETMY_M0_LOCK_L_OUT_DQ t=60s at 512Hz
2014-05-18 04:43:34 UTC (1084423430)

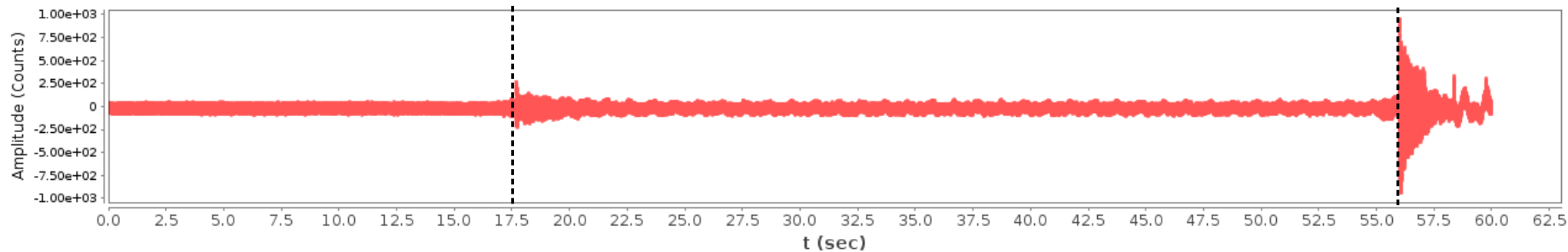
ISI-ETMX trip
DARM input shut down



H1:SUS-ETMY_L3_LOCK_L_OUT_DQ t=55s at 2048Hz
2014-05-18 04:43:34 UTC (1084423430)

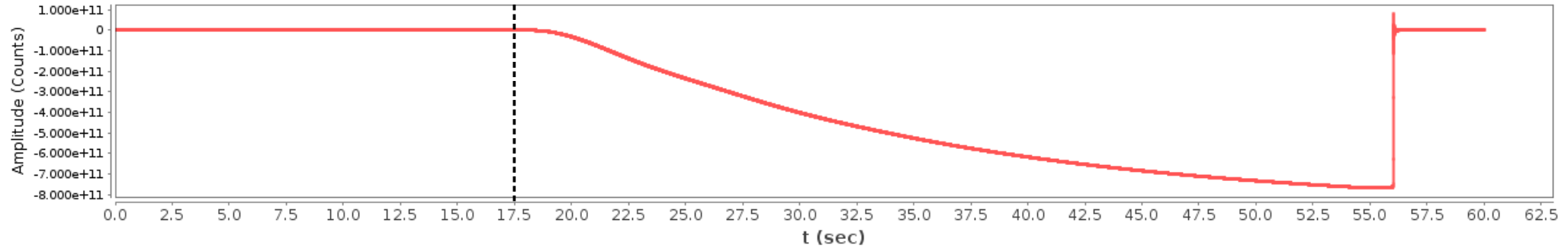


H1:ISI-ETMY_ST2_GS13INF_V1_IN1_DQ t=60s at 4096Hz
2014-05-18 04:43:34 UTC (1084423430)

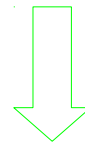


H1:ISI-ETMY_ST2_GS13INF_V1_IN1_DQ t=60s at 4096Hz
2014-05-18 04:43:34 UTC (1084423430)

**H1:LSC-DARM_CTRL_256_DQ t=60s at 256Hz
2014-05-18 04:43:34 UTC (1084423430)**

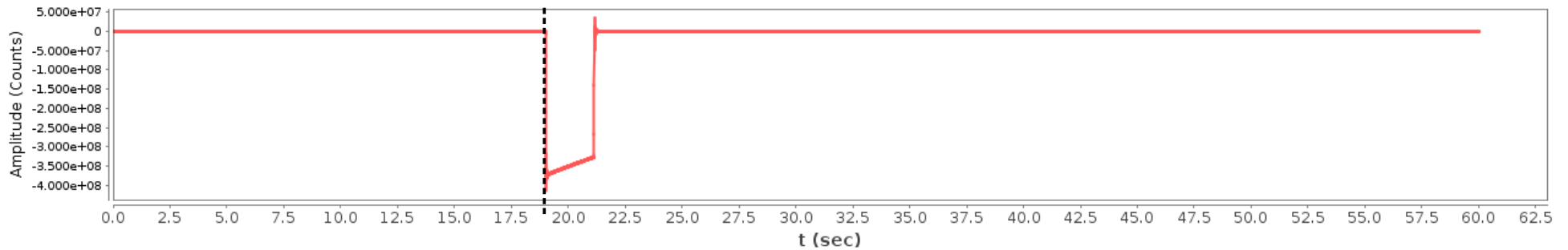


H1:LSC-DARM_CTRL_256_DQ t=60s at 256Hz
2014-05-18 04:43:34 UTC (1084423430)



New code

**H1:LSC-DARM_CTRL_256_DQ t=60s at 256Hz
2014-05-20 02:56:24 UTC (1084589800)**

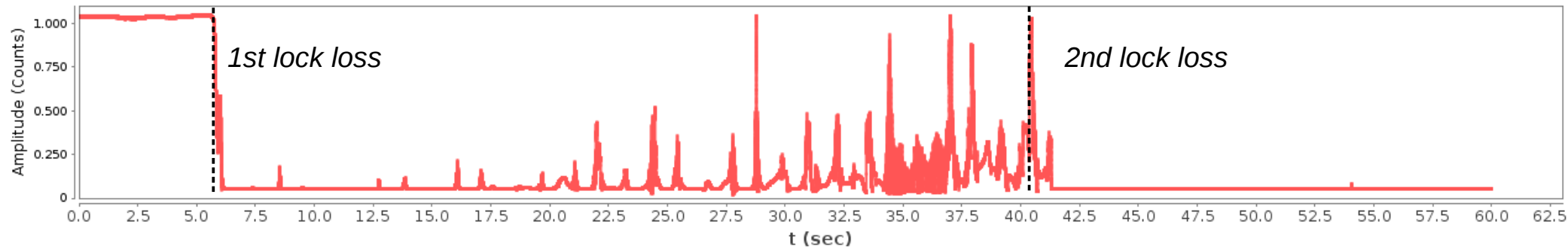


H1:LSC-DARM_CTRL_256_DQ t=60s at 256Hz
2014-05-20 02:56:24 UTC (1084589800)

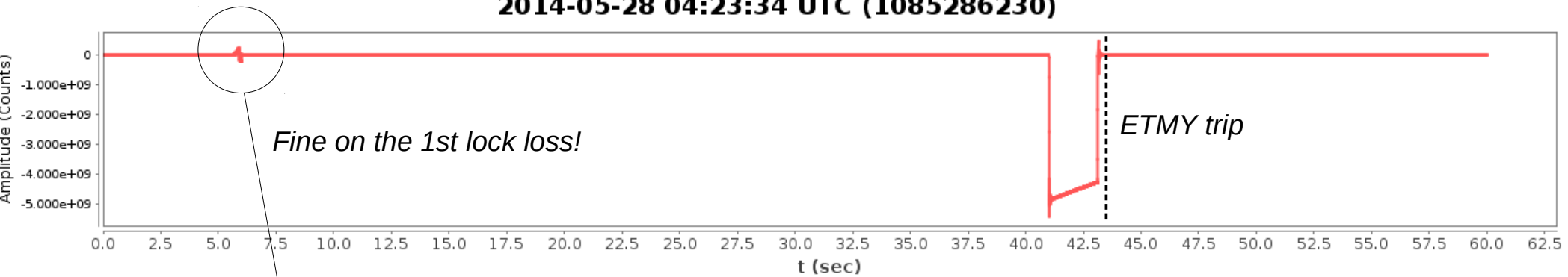
Not perfect, but L1/ETMX are not tripping anymore

Let's have a look at ETMY

H1:ALS-C_TRX_A_LF_OUT_DQ t=60s at 2048Hz
2014-05-28 04:23:34 UTC (1085286230)

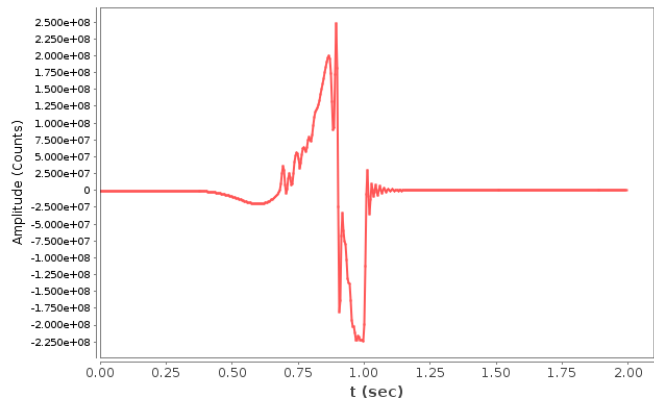


H1:LSC-DARM_CTRL_256_DQ t=60s at 256Hz
2014-05-28 04:23:34 UTC (1085286230)



H1:LSC-DARM_CTRL_256_DQ t=60s at 256Hz
2014-05-28 04:23:34 UTC (1085286230)

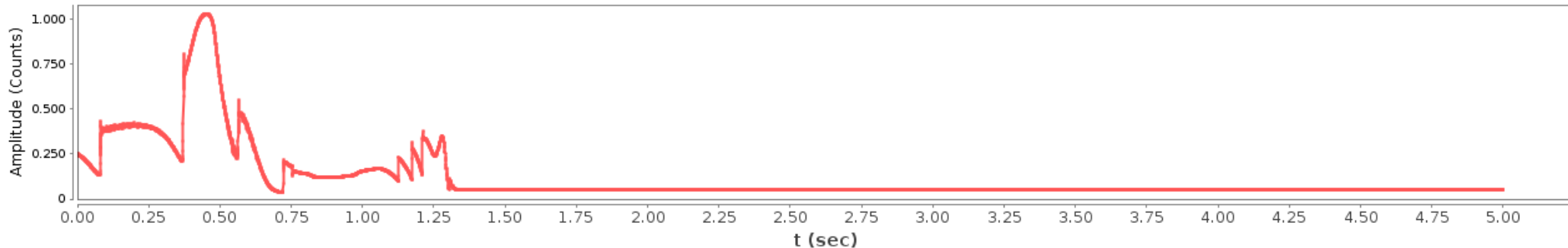
H1:LSC-DARM_CTRL_256_DQ t=2s at 256Hz
2014-05-28 04:23:39 UTC (1085286235)



H1:LSC-DARM_CTRL_256_DQ t=2s at 256Hz
2014-05-28 04:23:39 UTC (1085286235)

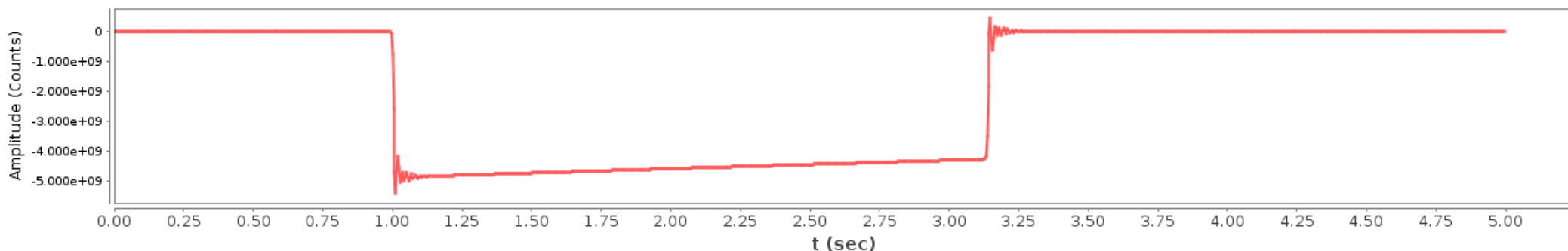
Let's focus on the 2nd lock loss

**H1:ALS-C_TRX_A_LF_OUT_DQ t=5s at 2048Hz
2014-05-28 04:24:14 UTC (1085286270)**



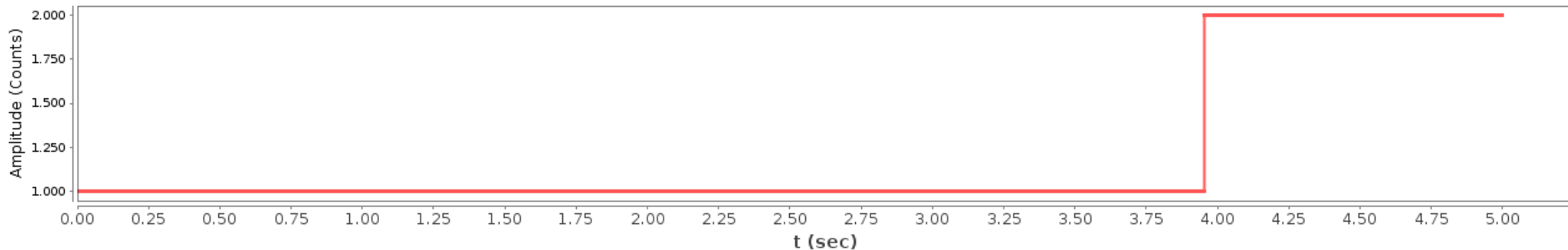
H1:ALS-C_TRX_A_LF_OUT_DQ t=5s at 2048Hz
2014-05-28 04:24:14 UTC (1085286270)

2014-05-28 04:24:14 UTC (1085286270)



H1:LSC-DARM_CTRL_256_DQ t=5s at 256Hz
2014-05-28 04:24:14 UTC (1085286270)

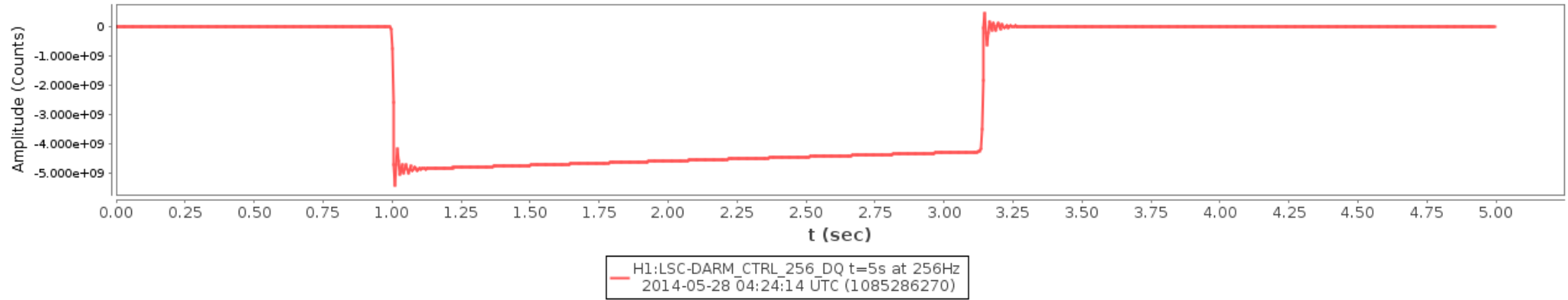
**H1:ISI-ETMY_ST2_WD_MON_STATE_IN1_DQ t=5s at 4096Hz
2014-05-28 04:24:14 UTC (1085286270)**



H1:ISI-ETMY_ST2_WD_MON_STATE_IN1_DQ t=5s at 4096Hz
2014-05-28 04:24:14 UTC (1085286270)

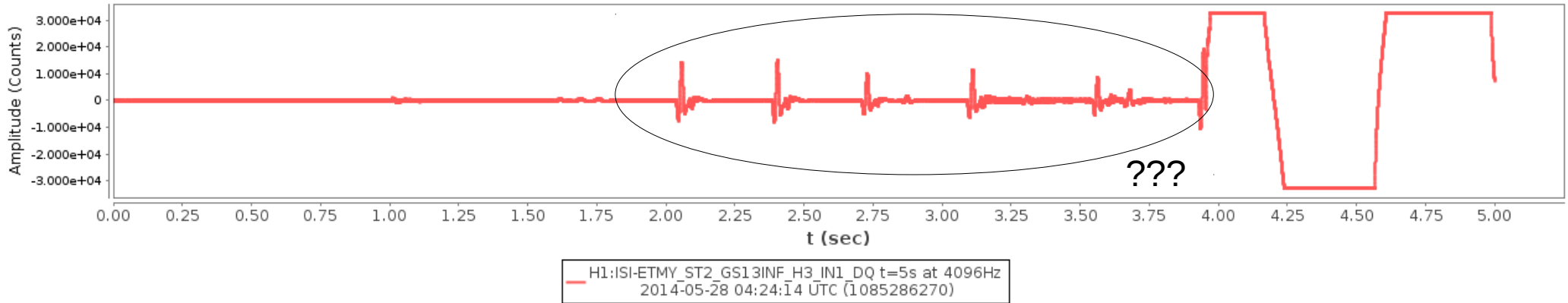
No trip on SUS

**H1:LSC-DARM_CTRL_256_DQ t=5s at 256Hz
2014-05-28 04:24:14 UTC (1085286270)**



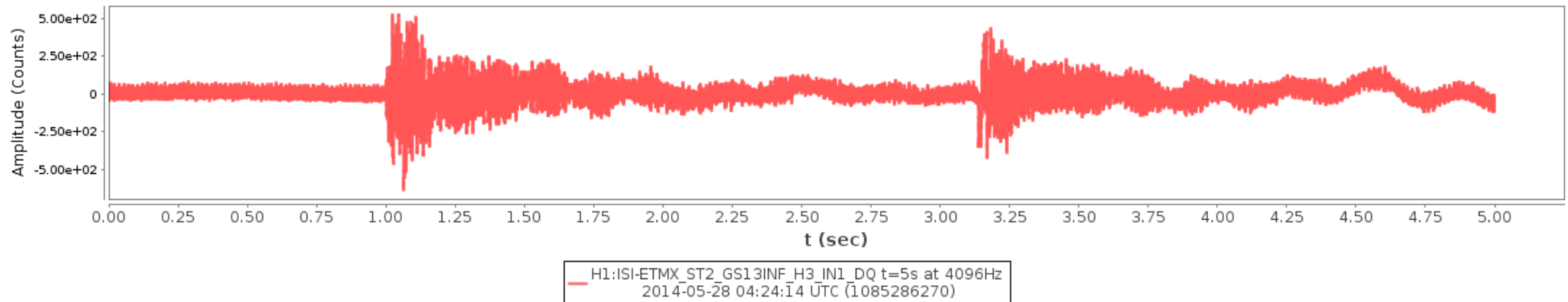
ETMY

**H1:ISI-ETMY_ST2_GS13INF_H3_IN1_DQ t=5s at 4096Hz
2014-05-28 04:24:14 UTC (1085286270)**

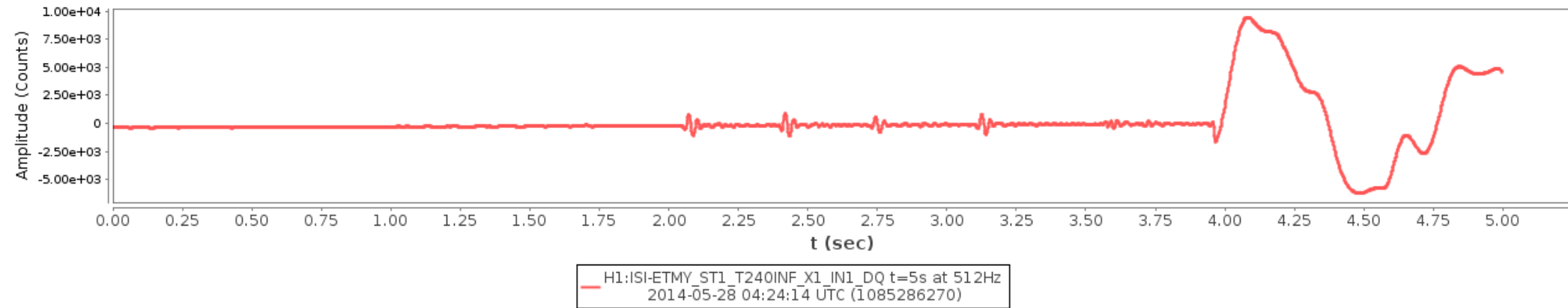


ETMX

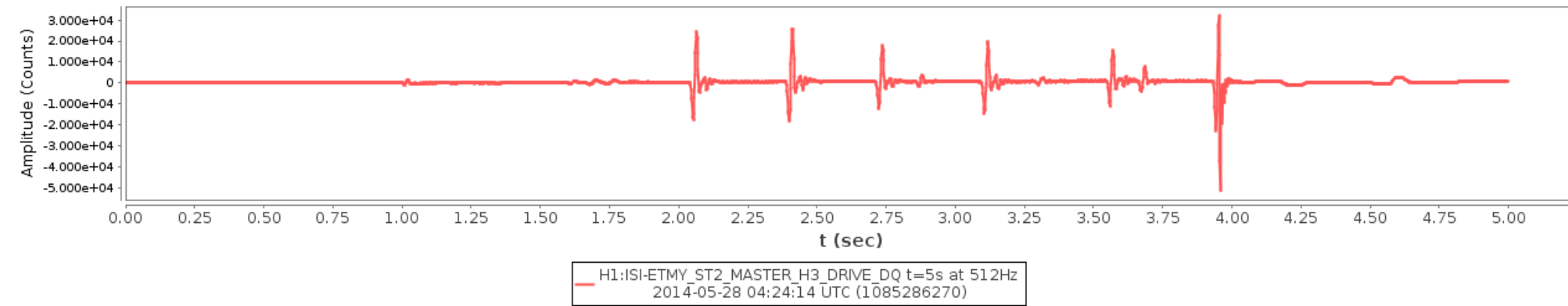
**H1:ISI-ETMX_ST2_GS13INF_H3_IN1_DQ t=5s at 4096Hz
2014-05-28 04:24:14 UTC (1085286270)**



**H1:ISI-ETMY_ST1_T240INF_X1_IN1_DQ t=5s at 512Hz
2014-05-28 04:24:14 UTC (1085286270)**

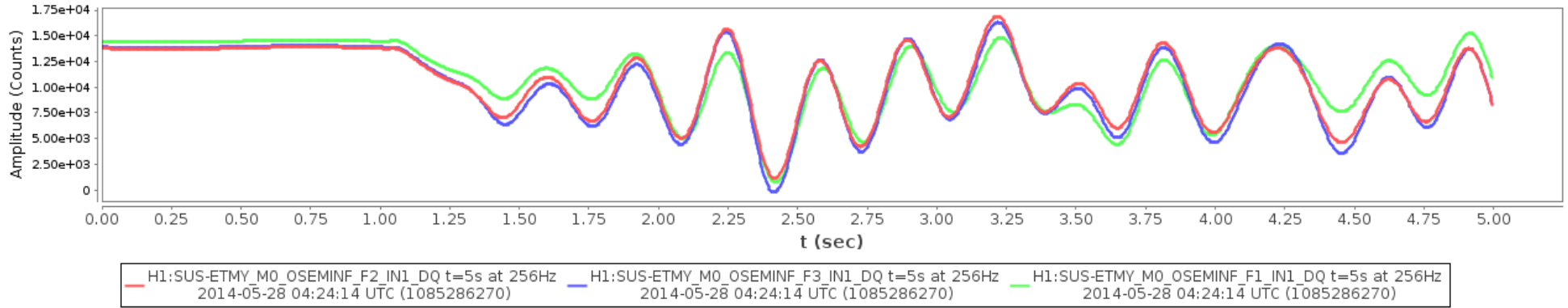


**H1:ISI-ETMY_ST2_MASTER_H3_DRIVE_DQ t=5s at 512Hz
2014-05-28 04:24:14 UTC (1085286270)**

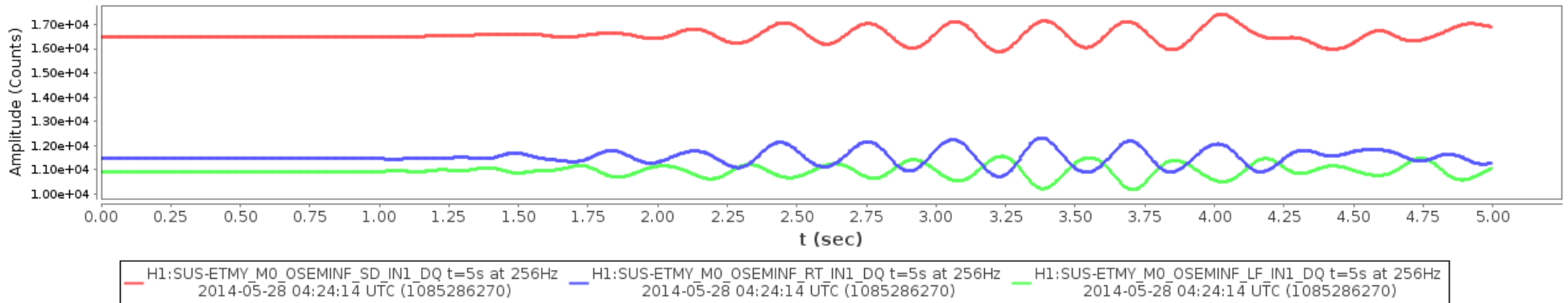


What about SUS?

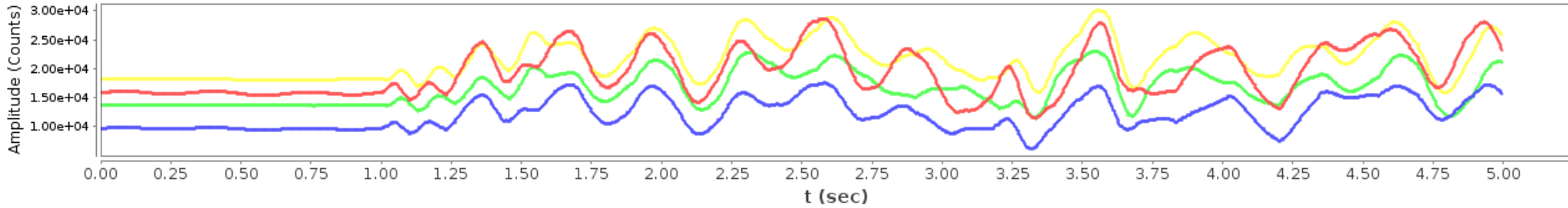
H1:SUS-ETMY_M0_OSEMINF_F1_IN1_DQ, H1:SUS-ETMY_M0_OSEMINF_F2_IN1_DQ, H1:SUS-ETMY_M0_OSEMINF_F3_IN1_DQ



H1:SUS-ETMY_M0_OSEMINF_LF_IN1_DQ, H1:SUS-ETMY_M0_OSEMINF_RT_IN1_DQ, H1:SUS-ETMY_M0_OSEMINF_SD_IN1_DQ

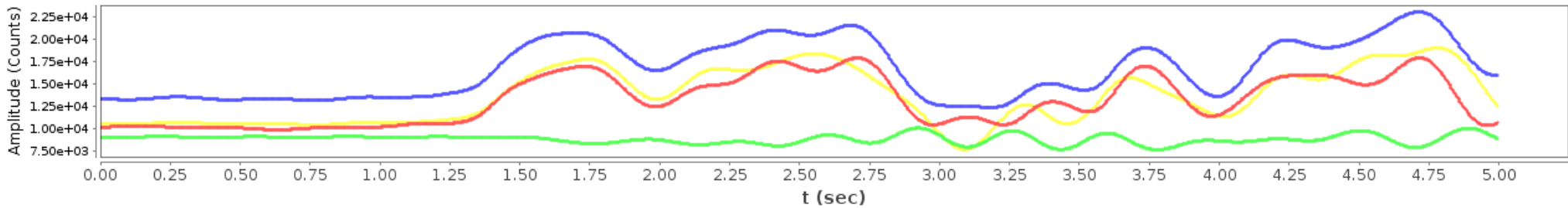


H1:SUS-ETMY_L1_OSEMINF_LL_IN1_DQ, H1:SUS-ETMY_L1_OSEMINF_LR_IN1_DQ, H1:SUS-ETMY_L1_OSEMINF_UL_IN1_DQ, H1:SUS-ETMY_L1_OSEMINF_UR_IN1_DQ



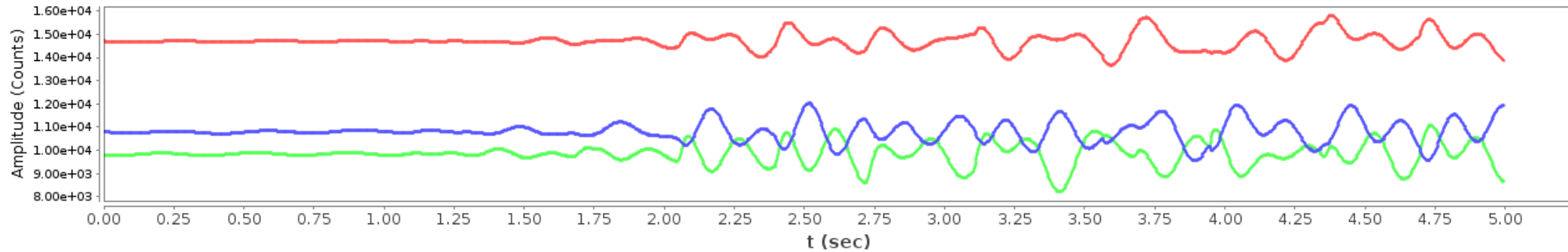
— H1:SUS-ETMY_L1_OSEMINF_LL_IN1_DQ t=5s at 256Hz 2014-05-28 04:24:14 UTC (I085286270)
 — H1:SUS-ETMY_L1_OSEMINF_LR_IN1_DQ t=5s at 256Hz 2014-05-28 04:24:14 UTC (I085286270)
 — H1:SUS-ETMY_L1_OSEMINF_UR_IN1_DQ t=5s at 256Hz 2014-05-28 04:24:14 UTC (I085286270)
 — H1:SUS-ETMY_L1_OSEMINF_UL_IN1_DQ t=5s at 256Hz 2014-05-28 04:24:14 UTC (I085286270)

H1:SUS-ETMY_L2_OSEMINF_LL_IN1_DQ, H1:SUS-ETMY_L2_OSEMINF_LR_IN1_DQ, H1:SUS-ETMY_L2_OSEMINF_UL_IN1_DQ, H1:SUS-ETMY_L2_OSEMINF_UR_IN1_DQ



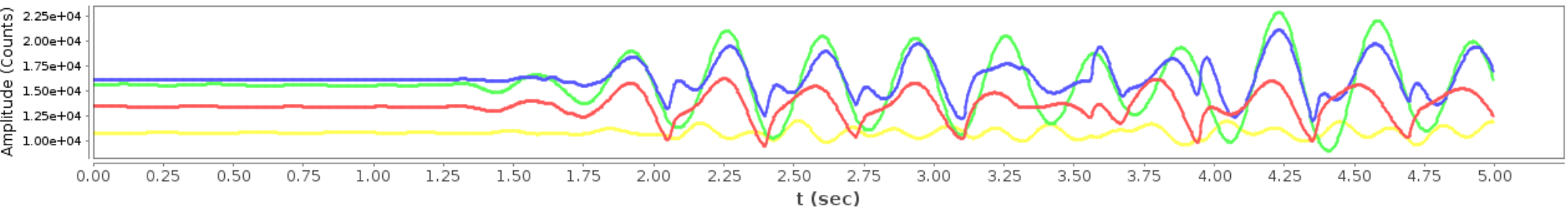
— H1:SUS-ETMY_L2_OSEMINF_UL_IN1_DQ t=5s at 256Hz 2014-05-28 04:24:14 UTC (I085286270)
 — H1:SUS-ETMY_L2_OSEMINF_LL_IN1_DQ t=5s at 256Hz 2014-05-28 04:24:14 UTC (I085286270)
 — H1:SUS-ETMY_L2_OSEMINF_UR_IN1_DQ t=5s at 256Hz 2014-05-28 04:24:14 UTC (I085286270)
 — H1:SUS-ETMY_L2_OSEMINF_LR_IN1_DQ t=5s at 256Hz 2014-05-28 04:24:14 UTC (I085286270)

H1:SUS-ETMY_R0_OSEMINF_LF_IN1_DQ, H1:SUS-ETMY_R0_OSEMINF_RT_IN1_DQ, H1:SUS-ETMY_R0_OSEMINF_SD_IN1_DQ



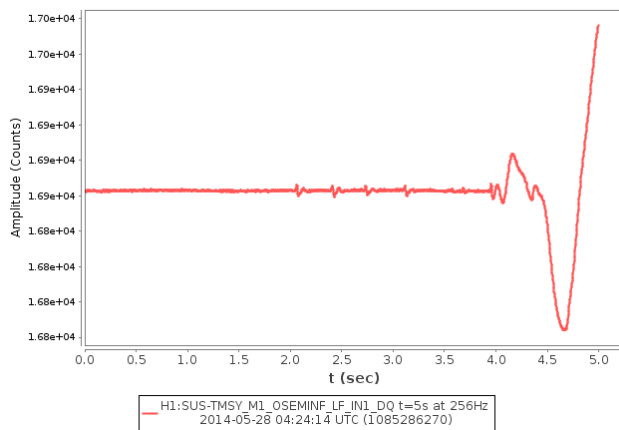
— H1:SUS-ETMY_R0_OSEMINF_SD_IN1_DQ t=5s at 256Hz 2014-05-28 04:24:14 UTC (I085286270)
 — H1:SUS-ETMY_R0_OSEMINF_LF_IN1_DQ t=5s at 256Hz 2014-05-28 04:24:14 UTC (I085286270)
 — H1:SUS-ETMY_R0_OSEMINF_RT_IN1_DQ t=5s at 256Hz 2014-05-28 04:24:14 UTC (I085286270)

H1:SUS-ETMY_R0_OSEMINF_F1_IN1_DQ, H1:SUS-ETMY_R0_OSEMINF_F2_IN1_DQ, H1:SUS-ETMY_R0_OSEMINF_F3_IN1_DQ, H1:SUS-ETMY_R0_OSEMINF_LF_IN1_DQ

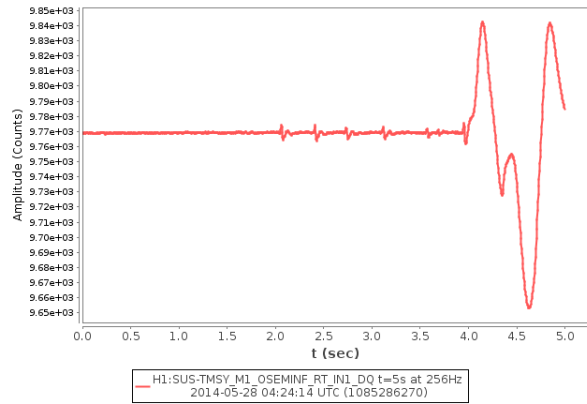


— H1:SUS-ETMY_R0_OSEMINF_F3_IN1_DQ t=5s at 256Hz 2014-05-28 04:24:14 UTC (I085286270)
 — H1:SUS-ETMY_R0_OSEMINF_F1_IN1_DQ t=5s at 256Hz 2014-05-28 04:24:14 UTC (I085286270)
 — H1:SUS-ETMY_R0_OSEMINF_F2_IN1_DQ t=5s at 256Hz 2014-05-28 04:24:14 UTC (I085286270)
 — H1:SUS-ETMY_R0_OSEMINF_LF_IN1_DQ t=5s at 256Hz 2014-05-28 04:24:14 UTC (I085286270)

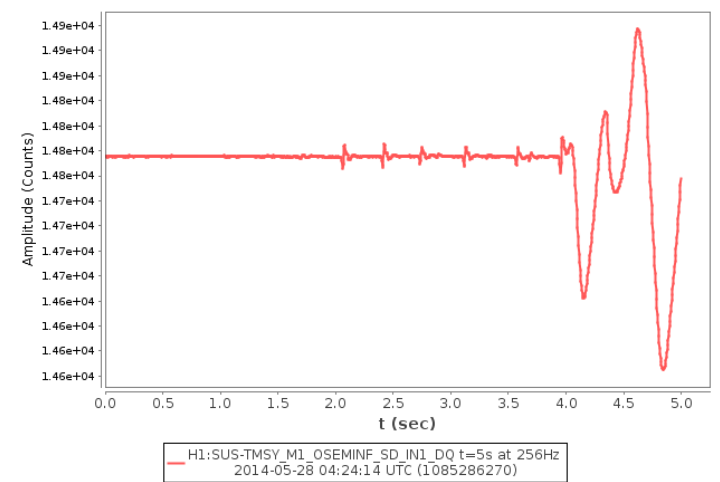
H1:SUS-TMSY_M1_OSEMINF_LF_IN1_DQ t=5s at 256Hz
2014-05-28 04:24:14 UTC (1085286270)



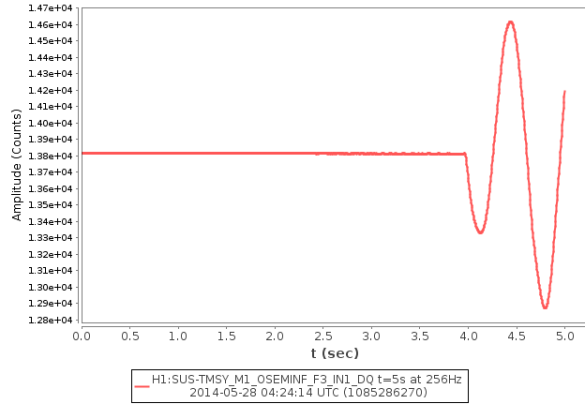
H1:SUS-TMSY_M1_OSEMINF_RT_IN1_DQ t=5s at 256Hz
2014-05-28 04:24:14 UTC (1085286270)



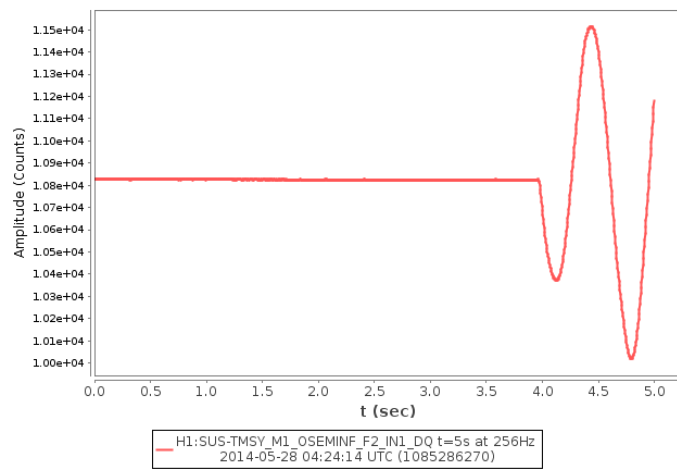
H1:SUS-TMSY_M1_OSEMINF_SD_IN1_DQ t=5s at 256Hz
2014-05-28 04:24:14 UTC (1085286270)



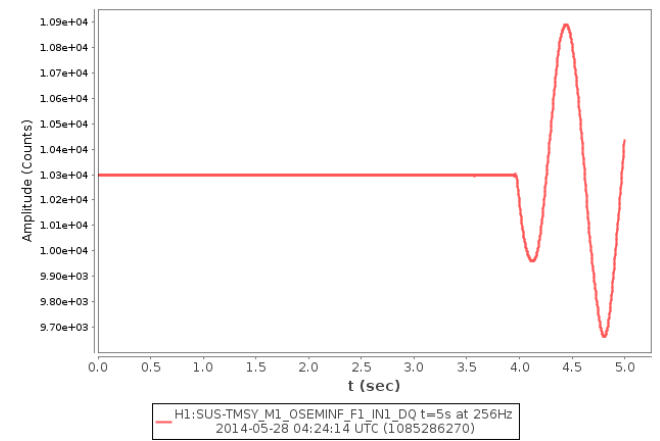
H1:SUS-TMSY_M1_OSEMINF_F3_IN1_DQ t=5s at 256Hz
2014-05-28 04:24:14 UTC (1085286270)



H1:SUS-TMSY_M1_OSEMINF_F2_IN1_DQ t=5s at 256Hz
2014-05-28 04:24:14 UTC (1085286270)

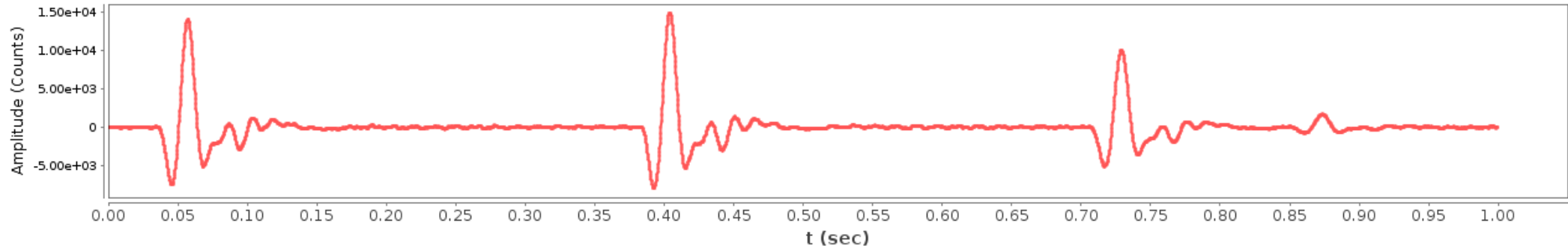


H1:SUS-TMSY_M1_OSEMINF_F1_IN1_DQ t=5s at 256Hz
2014-05-28 04:24:14 UTC (1085286270)

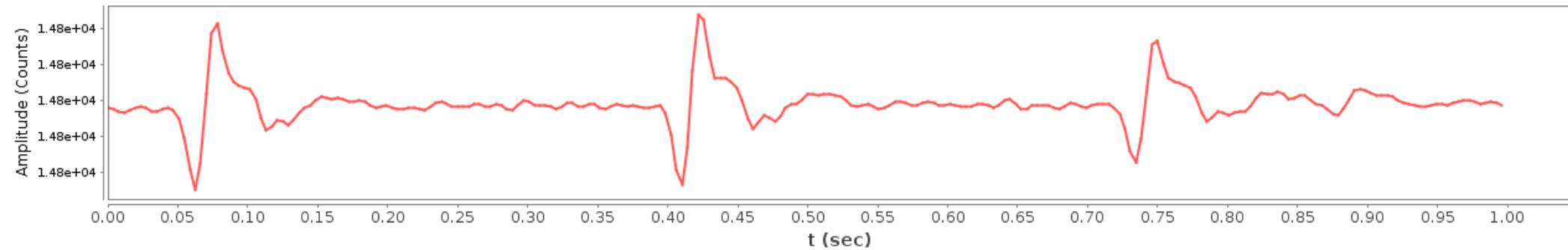


Shows up only on TMSY

**H1:ISI-ETMY_ST2_GS13INF_H3_IN1_DQ t=1s at 4096Hz
2014-05-28 04:24:16 UTC (1085286272)**



**H1:SUS-TMSY_M1_OSEMINF_SD_IN1_DQ t=1s at 256Hz
2014-05-28 04:24:16 UTC (1085286272)**



H1:SUS-TMSY_M1_OSEMINF_SD_IN1_DQ t=1s at 256Hz
2014-05-28 04:24:16 UTC (1085286272)

Need to investigate more on how the feedback signal is shut down

Does TMSY hit a stop when the platform is shaken around? What can we do about it?