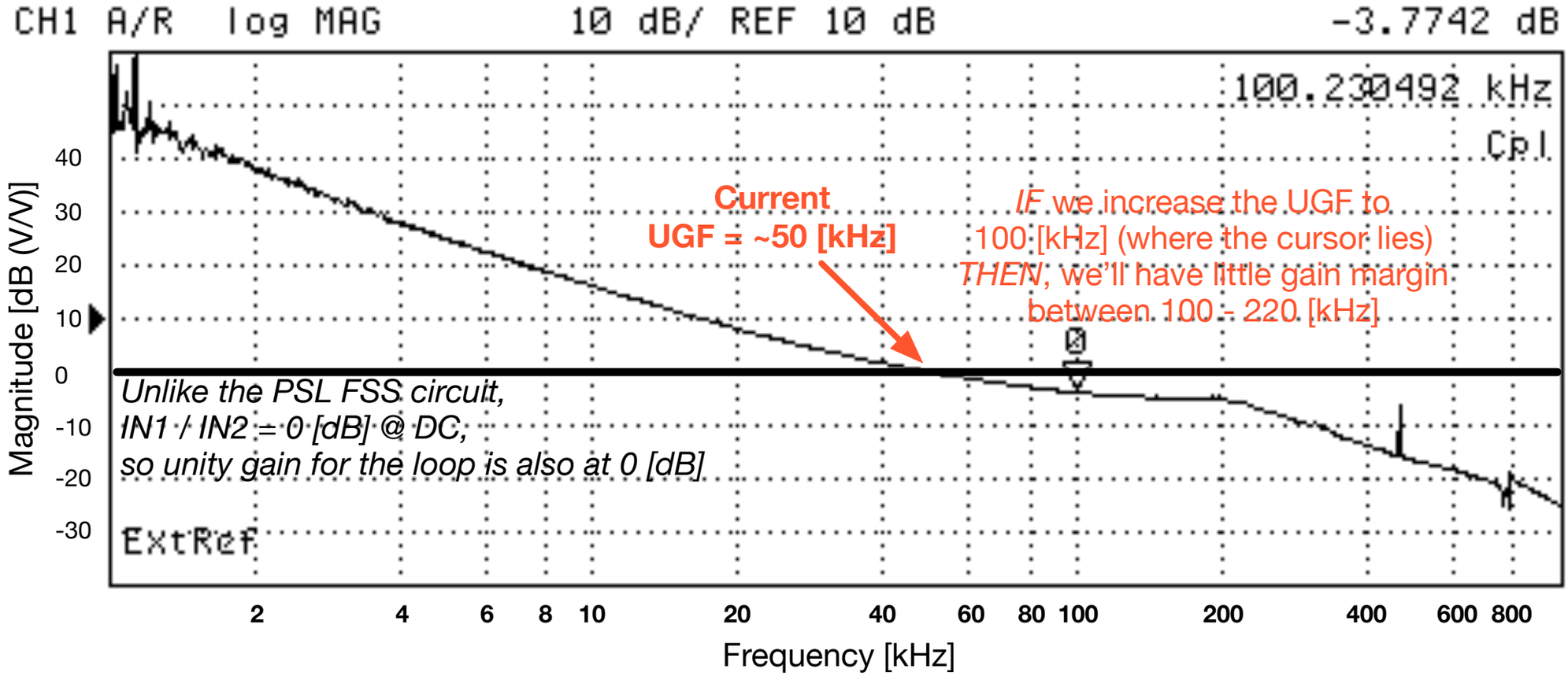
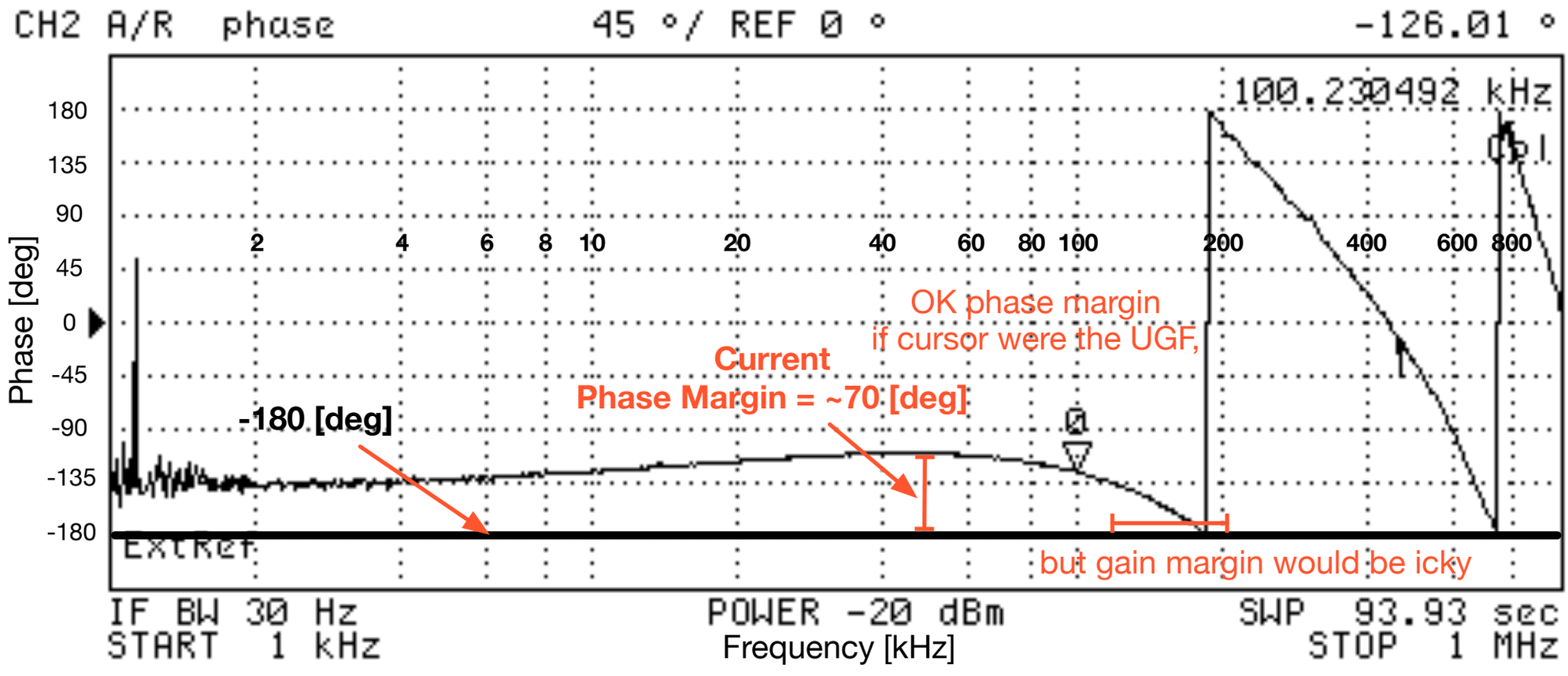

CH1 A/R log MAG 10 dB/ REF 10 dB -3.7742 dB
100.230492 kHz
Cpl
Current
UGF = ~50 [kHz]
IF we increase the UGF to
100 [kHz] (where the cursor lies)
THEN, we'll have little gain margin
between 100 - 220 [kHz]
Unlike the PSL FSS circuit,
IN1 / IN2 = 0 [dB] @ DC;
so unity gain for the loop is also at 0 [dB]
ExtRef
Magnitude [dB (V/V)]
40
30
20
10
0
-10
-20
-30
2
4
6
8
10
20
40
60
80
100
200
400
600
800
Frequency [kHz]


CH2 A/R phase 45 °/ REF 0 ° -126.01 °
100.230492 kHz
Cpl
Phase [deg]
180
135
90
45
0
-45
-90
-135
-180
2
4
6
8
10
20
40
60
80
100
200
400
600
800
OK phase margin
if cursor were the UGF,
Current
Phase Margin = ~70 [deg]
-180 [deg]
ExtRef
but gain margin would be icky
IF BW 30 Hz
START 1 kHz
POWER -20 dBm
Frequency [kHz]
SWP 93.93 sec
STOP 1 MHz