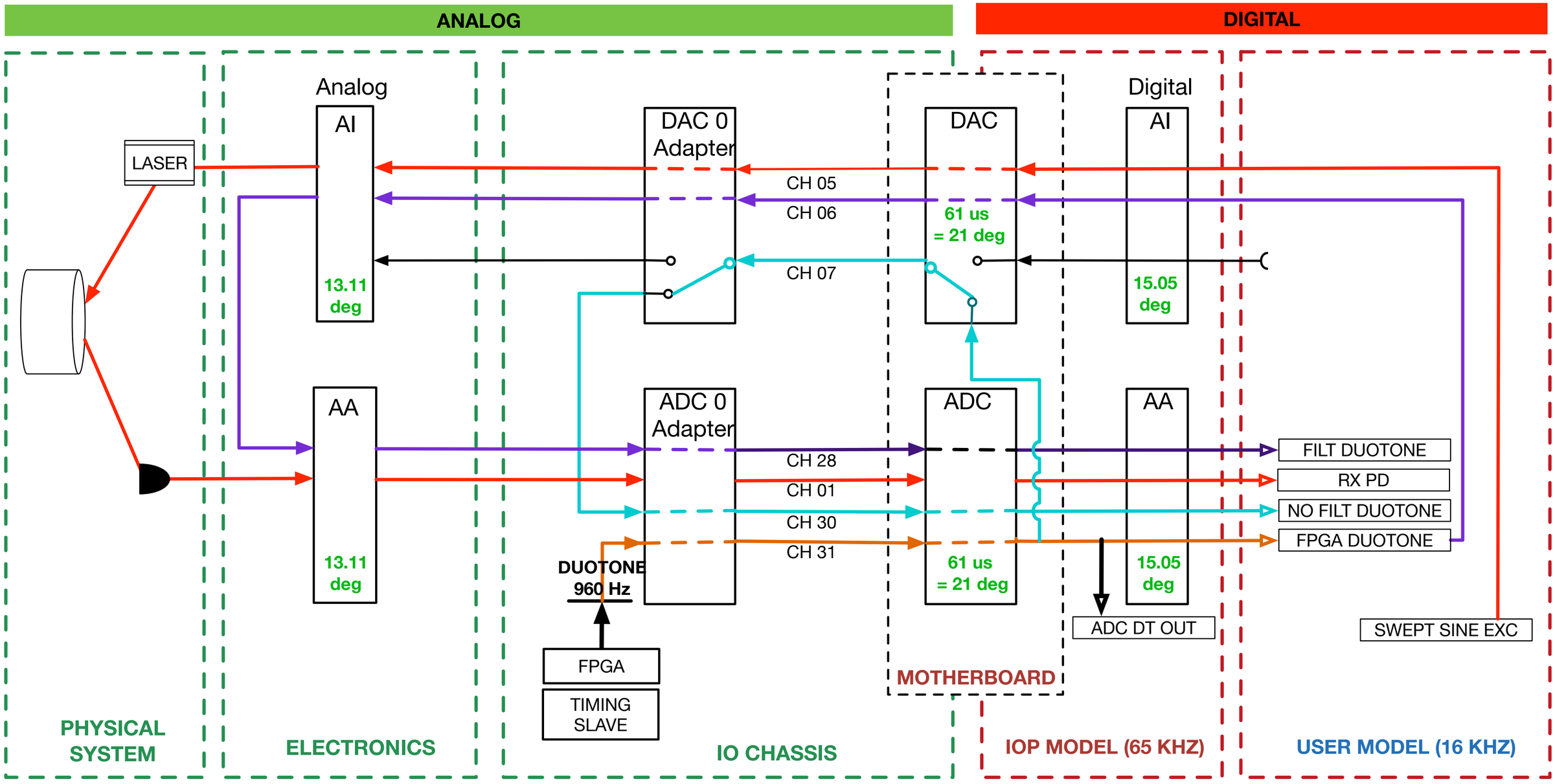
LHO aLOG 28942

SCHEMATICS OF PCAL TIMING SIGNALS



All phases referenced at 960 Hz

			Measured Phase (deg)	Measured Delta Phase From 219.4 (deg)	Modeled Delta Phase (deg)
SWEPT SINE EXC	H1:CAL-PCALY_SWEPT_SINE_EXC	T=0	219.4	—	
ADC DT OUT	H1:IOP-ISC_EY_ADC_DT_OUT	T=0	218.6	—	
FPGA DUOTONE	H1:CAL-PCALY_FPGA_DTONE_IN1	T=0	203.8	15.6	15 deg (AAD)
NO FILT DUOTONE	H1:CAL-PCALY_DAC_NONFILT_DTONE_IN1	T=1	182.7	36.7	36 deg = 21 deg (61 us delay) + 15 deg (AAD)
FILT DUOTONE	H1:CAL-PCALY_DAC_FILT_DTONE_IN1	T=2	100.2	119.2	98 deg = 15 deg (AID) + 21 deg (61 us delay) + 13 deg (AIA) + 13 deg (AAA) + 21 (61 us delay) + 15 deg (AAD)
RX PD	H1:CAL-PCALY_RX_PD_VOLTS_OUT	T=2	96.4	123	98 deg = 15 deg (AID) + 21 deg (61 us delay) + 13 deg (AIA) + 13 deg (AAA) + 21 (61 us delay) + 15 deg (AAD)