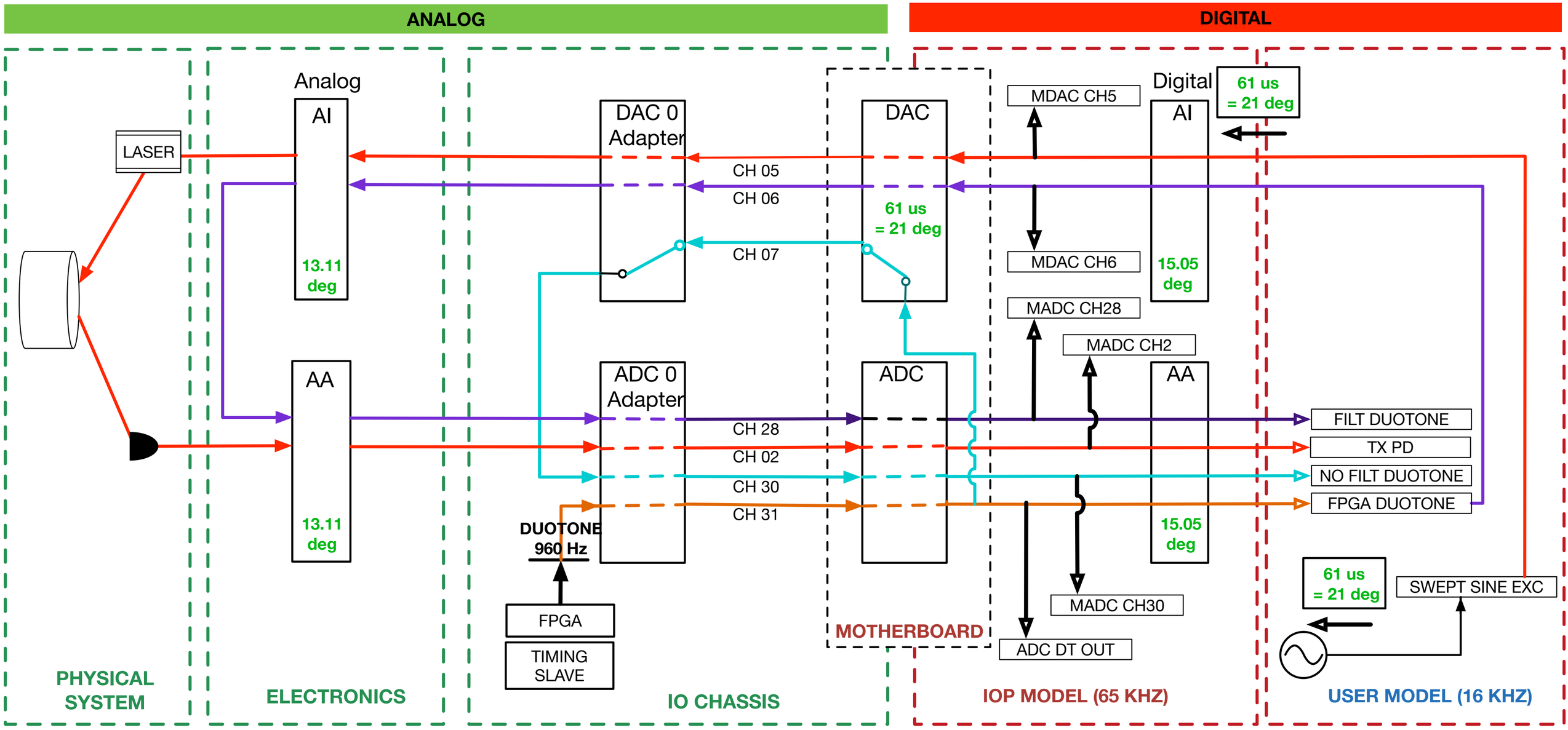
LHO aLOG 29259

SCHEMATICS OF PCAL TIMING SIGNALS



All phases referenced at 960 Hz

		Measured Delta Phase From ADC_DT_OUT (deg)	Measured Delta Phase From SINE_OUT (deg)	Modeled Delta Phase (deg)
ADC DT OUT	H1:IOP-ISC_EX_ADC_DT_OUT	—	—	
FPGA DUOTONE	H1:CAL-PCALX_FPGA_DTONE_IN1	-15.05	—	-15 deg (AAD)
MDAC CH6	H1:IOP-ISCEX_MDAC0_TP_CH6	-51.2	—	-52 deg = 21 deg (61 us delay) + 15 deg (AAD) + 15 deg (AID)
MADC CH28	H1:IOP-ISC_EX_MADC0_TP_CH28	-100.07	—	-98 deg = 21 deg (61 us delay) + 15 deg (AAD) + 15 deg (AID) + 13 deg (AIA) + 13 deg (AAA) + 21 deg (61 us delay)
FILT DUOTONE	H1:CAL-PCALY_DAC_FILT_DTONE_IN1	-115.13	—	-113 deg = 21 deg (61 us delay) + 15 deg (AAD) + 15 deg (AID) + 13 deg (AIA) + 13 deg (AAA) + 21 deg (61 us delay) + 15 deg (AAD)
MADC CH30	H1:IOP-ISC_EX_MADC0_TP_CH30	-21.29	—	-21 deg (61 us delay)
NO FILT DUOTONE	H1:CAL-PCALY_DAC_NONFILT_DTONE_IN1	-36.35	—	-36 deg = 21 deg (61 us delay) + 15 deg (AAD)
SWEPT SINE EXC	H1:CAL-PCALY_SWEPT_SINE_EXC	—	—	(Note: user model excitations have a 21 deg advance)
MDAC CH5	H1:IOP-ISCEX_MDAC0_TP_CH5	—	-36.15	-36 deg = 21 deg (61 us delay) + 15 deg (AID)
MADC CH2	H1:IOP-ISC_EX_MADC0_TP_CH2	—	-85.25	-83 deg = 21 deg (61 us delay) + 15 deg (AID) + 13 deg (AIA) + 13 deg (AAA) + 21 deg (61 us delay)
RX PD	H1:CAL-PCALY_RX_PD_VOLTS_OUT	—	-100.3	-98 deg = 21 deg (61 us delay) + 15 deg (AID) + 13 deg (AIA) + 13 deg (AAA) + 21 deg (61 us delay) + 15 deg (AID)