**OMC DCPD Signal Timing Diagram**
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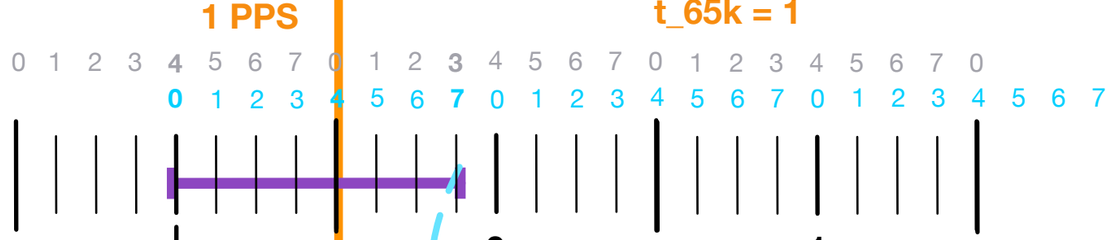
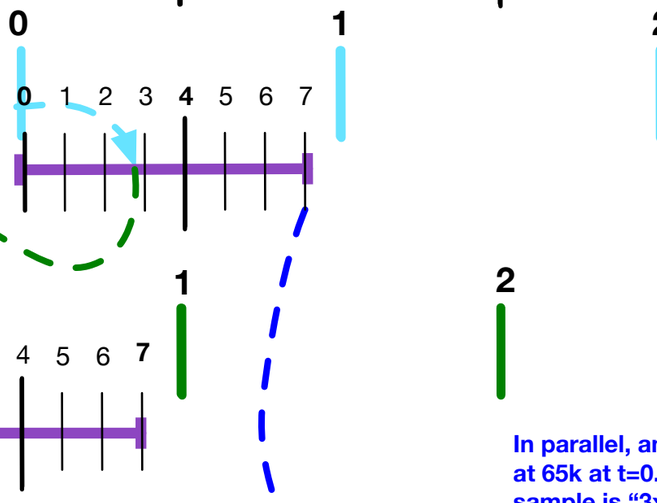
8x 524 kHz ADC voltage points are read in all at once by beginning of the 8th sample, 7, by the 65 kHz process. These points are chose to be 4 points “in the future,” “4” points “in the past” w.r.t. t=0.

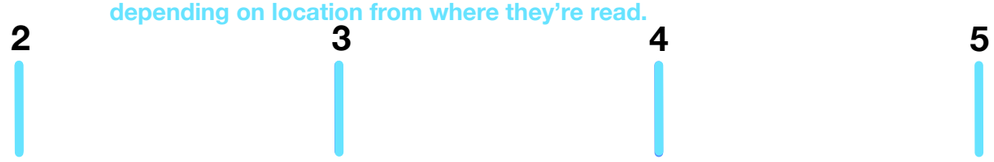
BUT, the read, filtering, and decimation all happen within a few 524 kHz clock cycles after that 8th sample is available, and the eventual answer is stored by the 65 kHz process at various time-stamps, causing discrepant delays between channels, depending on location from where they’re read.




**524 kHz** ADC Voltage Samples

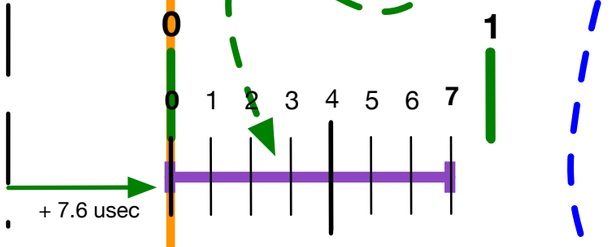
**65 kHz** process, Starts 4x 524 kHz cycles behind t=0




The 65k IOP process stores all 8x 524k computations in 524k test points “at 524 kHz” with the *first* 524k sample, 0, stamped with t=0 PPS. Thus, each data point of a “524k data” channel has 4 / 524 kHz = 7.6 usec of delay from when the voltage as sampled by the ADC.

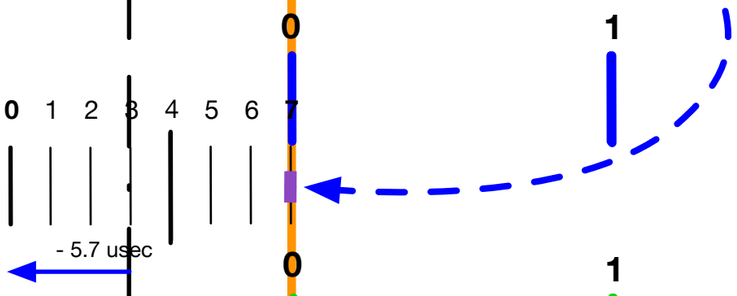
**65 kHz** IOP Test Point Write for DAQ/NDS as “524 kHz”





In parallel, and differently, the 8th 524k data point, 7, is posted for direct user model pick-up as “ADC Out” at 65k at t=0. Thus, the *last* 524k sample, is now representing the t=0 65k data point, and the *first* 524k sample is “3x 524 kHz cycles in the future of when the ADC volts were sampled” or *advanced* by - 3 / 524 kHz = - 5.7 usec. If 16k user model consumes this directly, its test point channels will have this advance.

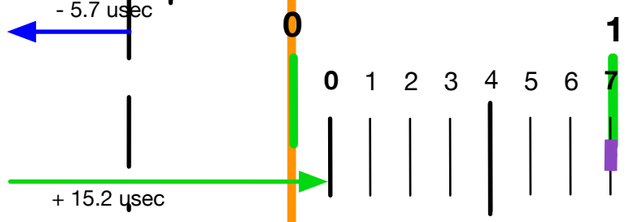
**65 kHz** write to “ADC Out” for user models





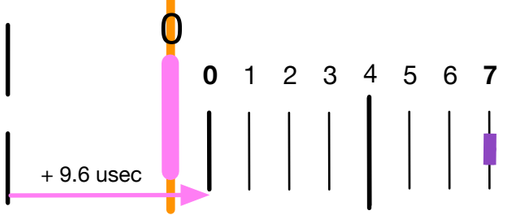
If the data is sent over to the via IPC, *all* 524k samples acquire 1 / 65 kHz = 8 / 524 kHz = 15.2 usec delay, because RCG stamps 65k IPC data with t=1.

**65 kHz** IPC time stamps data at t=1





**16 kHz** OMC Test Point Write for DAQ/NDS





The value of the 8th 524k sample is used for the entire 16k cycle, stamped at t=0. So *first* (and all subsequent) 524k samples is (are) now at ( -3x + 8x ) = 5x 524k samples = 9.6 usec of delay w.r.t. when it was read by the ADC.